

FIG. 1

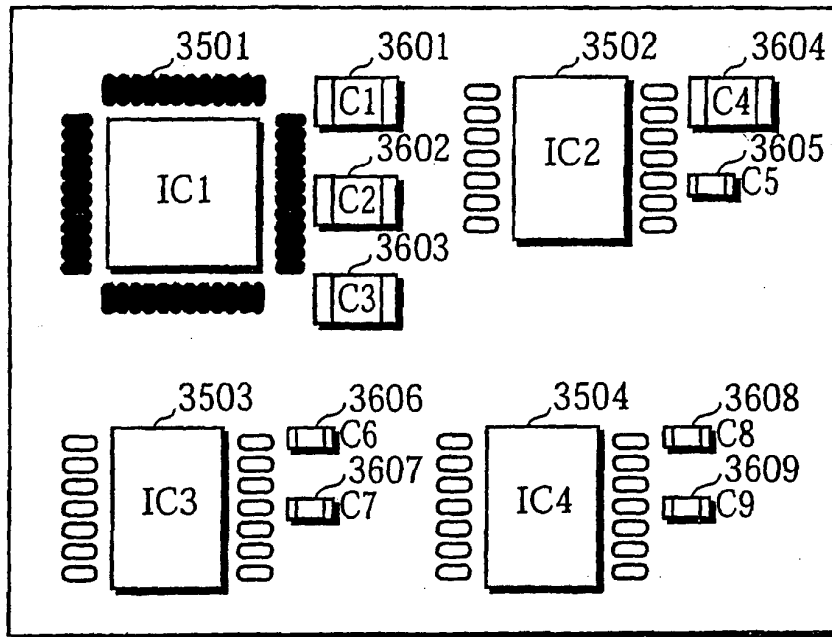


FIG. 2

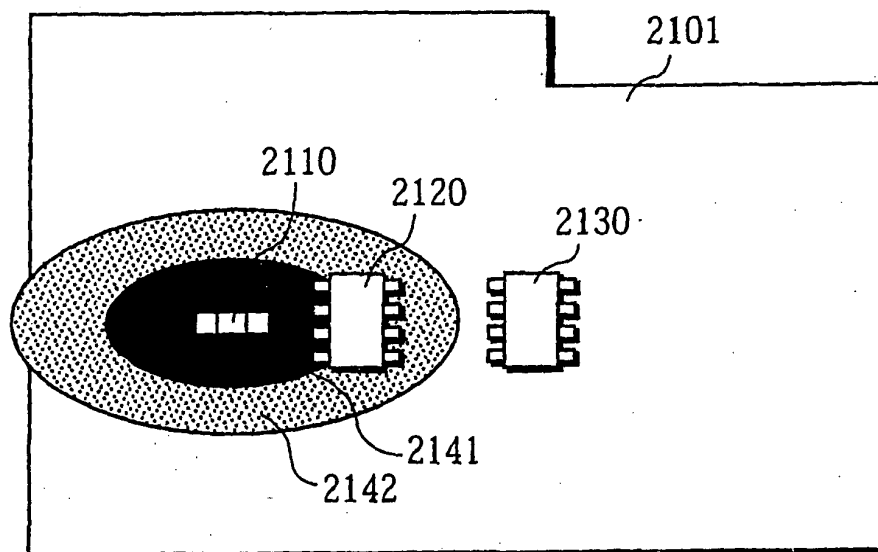


FIG. 3

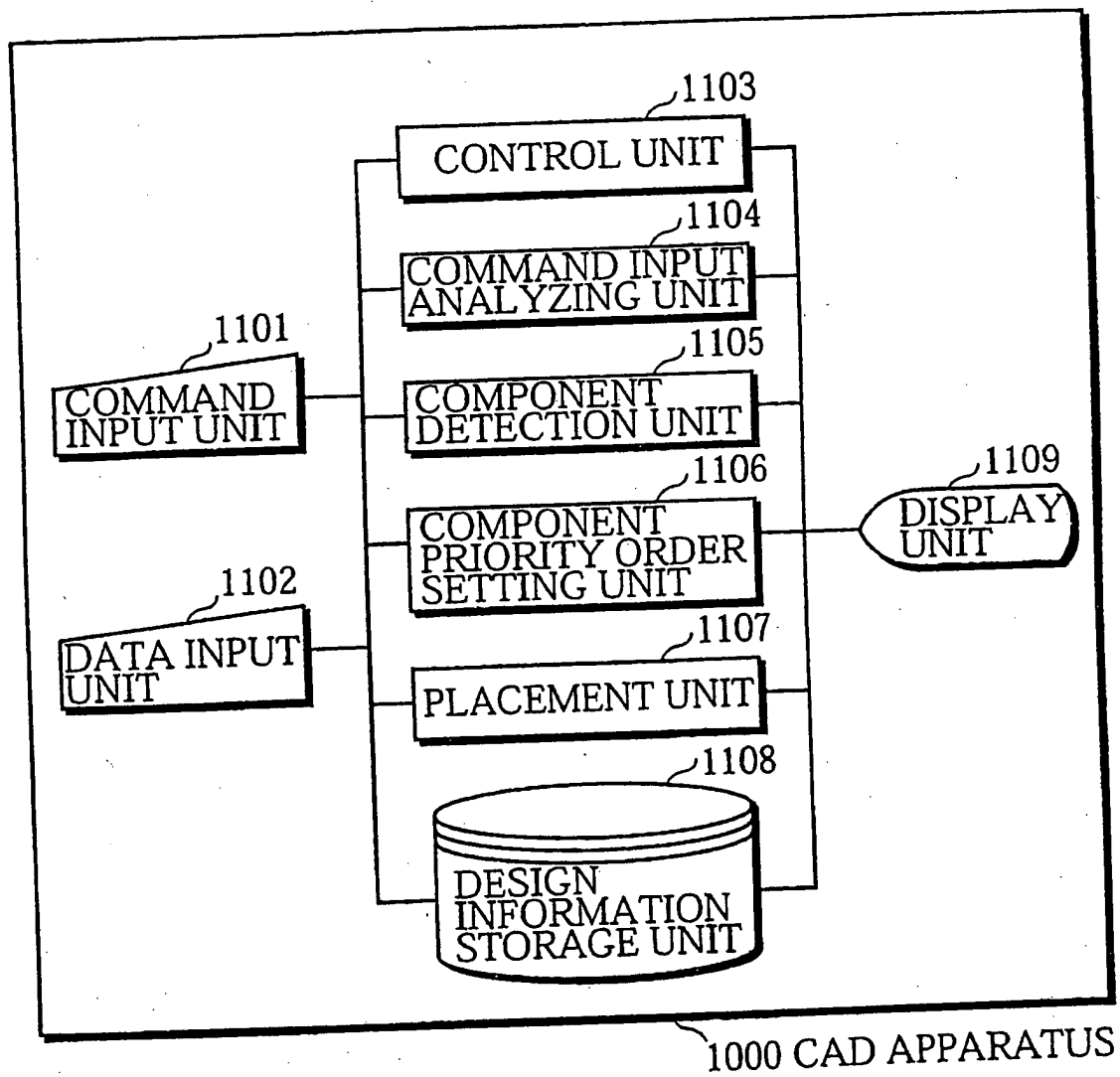


FIG. 4

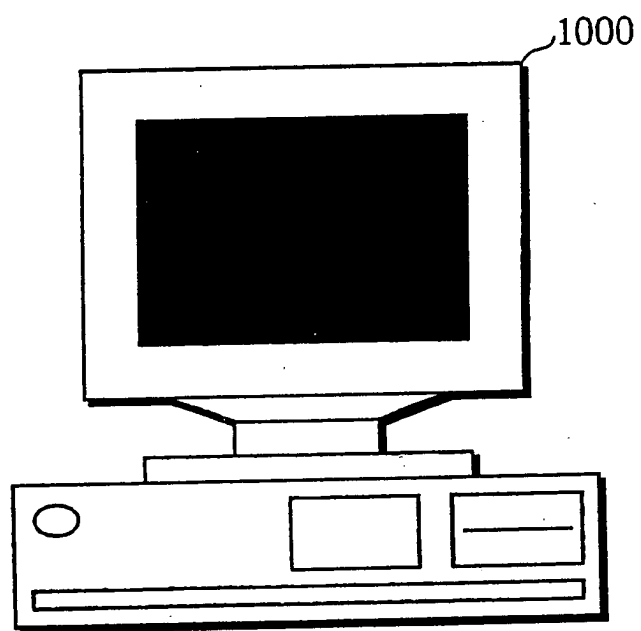


FIG. 5

1201 COMPONENT INFORMATION LIST

1202	1203	1204	1205	1206	1207	1208	1209	1210
COMPONENT NUMBER	COMPONENT NAME	COMPONENT SHAPE	PLACEMENT SURFACE	BASE POINT COORDINATES	PRIORITY ORDER	MAIN COMPONENT NUMBER	AUXILIARY COMPONENT NUMBER	COMPONENT GROUP
IC1	MN1	QFP1	A	(132,135)	-	-	C1,C5,C6,C10 L1	1
IC2	MN2	SOP1	A	(46,123)	-	-	C2,C7,R1	1
IC3	MN3	SOP1	A	(32,45)	-	-	C3,C8	1
...
C1	EC1	SOP11	A	(143,120)	28	IC1	-	2
C2	EC1	SOP11	A	(50,101)	28	IC2	-	2
C3	EC1	SOP11	A	(28,30)	28	IC3	-	2
...
1220	1221	1224	1232	1233	1234	1223	1222	
1230	1231	1232	1232	1233	1234	1223	1222	

FIG. 6

1301 COMPONENT MASTER INFORMATION LI

1302	1303	1304	1305	1306	1307	1308	1309	1310
COMPONENT NAME	PIN COUNT	COMPONENT TYPE	L VALUE [nH]	C VALUE [uF]	R VALUE [Ω]	INTERNAL CLOCK-POWER NET NAME	EFFECTIVE FREQUENCY MIN [MHz]	EFFECTIVE FREQUENCY MAX [MHz]
MN1	IC	48	-	-	-	33MHz-vcc2	-	-
MN2	IC	14	-	-	-	-	-	-
MN3	IC	14	-	-	-	-	-	-
...
EC1	C	2	1.1	10	0.1	-	0	50
EC2	C	2	0.8	0.1	0.1	-	0	200
EC3	C	2	0.6	0.01	0.1	-	0	500
...

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FIG. 7

1401 NET INFORMATION LIST

1402	1403	1404	1405	1406	1407	1408	1409	1410
NET INFORMATION LIST	CONTACT PIN NUMBER (COMPONENT NUMBER, PIN NUMBER)	FREQUENCY [MHz]	RISING TIME [ns]	FALLING TIME [ns]	OUTPUT VOLTAGE HIGH [V]	OUTPUT VOLTAGE LOW [V]	NET TYPE	DUTY RATIO
clk1	IC1-2,R1-1	30	1.4	1.35	3.3	0.0	clock	0.48
clk3	IC1-20,IC2-2 IC3-2,IC4-2	16	1.5	1.48	3.3	0.0	clock	0.49
n1	IC1-1,IC2-3	—	—	—	—	—	—	—
n101	R1-2,IC4-12	30	1.4	1.35	3.3	0.0	clock	0.48
v1	IC1-4,IC1-6, IC2-6,IC2-10 C1-1,C2-1,C3-1	—	—	—	—	—	power	—
...

1423

1422

1421

FIG. 8

1501 PIN INFORMATION LIST

1502	1503	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517
COMPONENT NUMBER	PIN NUMBER	PIN NAME	POWER NET NAME	POWER PIN NUMBER	FREQUENCY [MHz]	RISING TIME [ns]	FALLING TIME [ns]	OUTPUT VOLTAGE HIGH [V]	OUTPUT VOLTAGE LOW [V]	PRIORITY ORDER	USAGE FREQUENCY MIN [MHz]	USAGE FREQUENCY MAX [MHz]	PIN TYPE	CONSUMED CURRENT [mA]	DUTY RATIO
IC1	1	p1	-	-	-	-	-	-	-	-	-	-	normal	-	-
IC1	2	clk	v1	4	30	1.4	1.35	3.3	0.0	-	0	300	clock	-	0.49
IC1	4	v1	-	-	30	1.4	1.35	3.3	0.0	1	0	300	power	10	-
IC1	6	v1	-	-	15	1.5	1.48	3.3	0.0	2	0	200	power	20	-
IC1	20	clk3	v1	18	15	1.5	1.48	3.3	0.0	-	0	200	clock	-	0.48
IC1	47	v2	-	-	33	1.0	0.9	2.0	0.0	1	0	400	power	20	-
...

1530 1531 1533 1534 1535 1536 1537 1538 1539 1540 1541
 1551 1532 1555 1556 1557 1558 1559 1560

FIG. 9

1601 EFFECTIVE FREQUENCY SPECTRUM
INFORMATION LIST

1602 PIN SPACING [mm]	1603 INDUCTANCE VALUE [nH]	1604 EFFECTIVE FREQUENCY SPECTRUM [MHz]
0-0.5	0.8	(0.1-500)
0.5-1.0	0.9	(0.1-300)
1.0-1.5	1.1	(0.1-100)
1.5-2.0	1.2	(0.1-100)
...

1610

1611

1612

FIG. 10

1701 COMPONENT SHAPE INFORMATION LIST

1702	1703	1704	1705	1706
COMPONENT SHAPE	MINIMUM/MAXIMUM DOMAIN	PIN NUMBER	PIN COORDINATES	PIN SPACING [mm]
QFP1	(0,0) - (15,15)	1	(0,3,0,3)	0.2
		2	(0,3,0,5)	
		
BGA1	(0,0) - (13,13)	1	(0,2,0,2)	0.2
		2	(0,2,0,4)	
		
SOP1	(0,0) - (10,15)	1	(0,2,0,2)	0.2
		2	(0,2,0,4)	
		
...
SOP11	(0,0) - (10,0.5)	1	(0,15,0,25)	0.7
		2	(0,85,0,25)	
...

1710

1711
1712

1713

FIG. 11

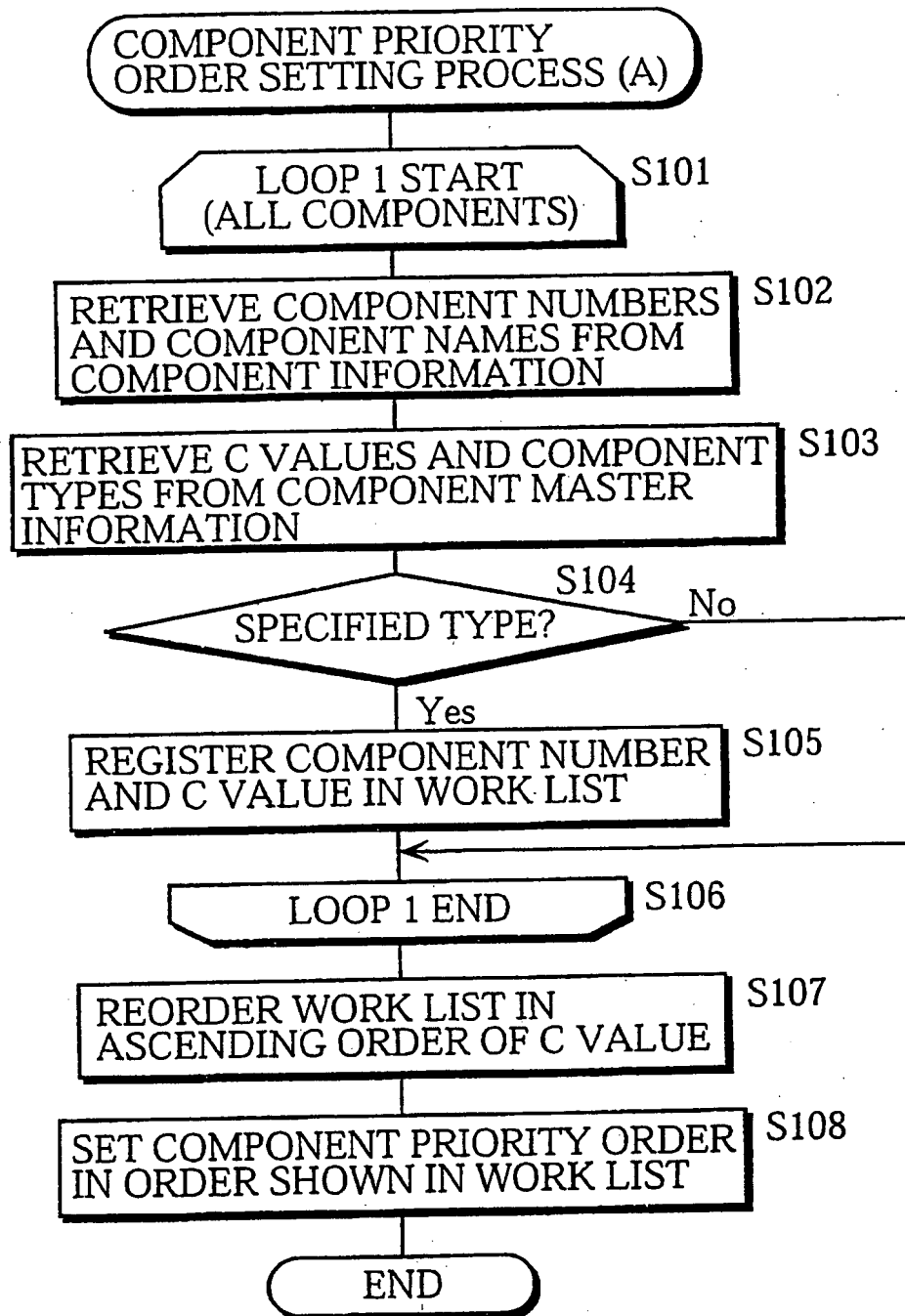


FIG. 12

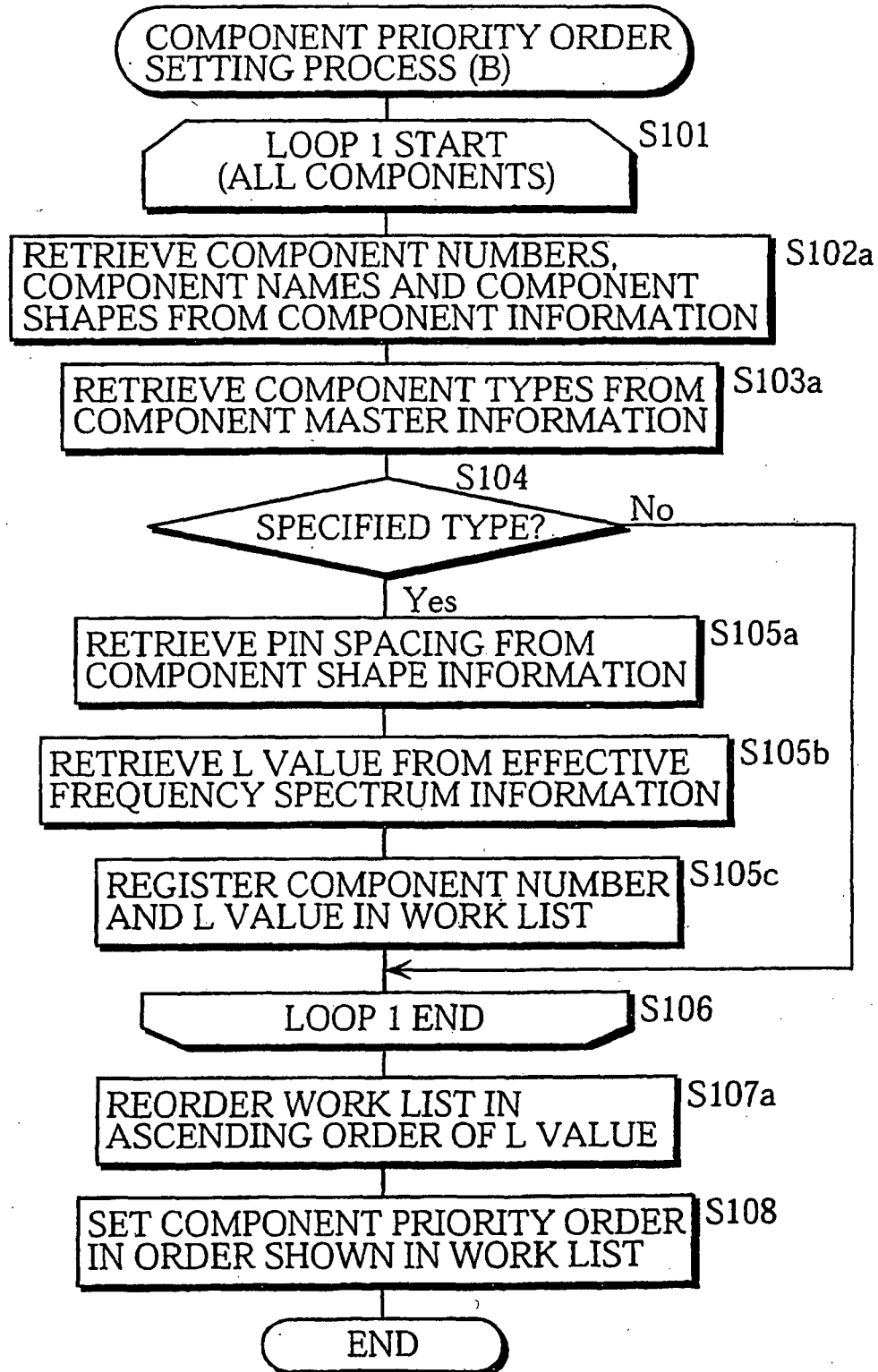


FIG. 13

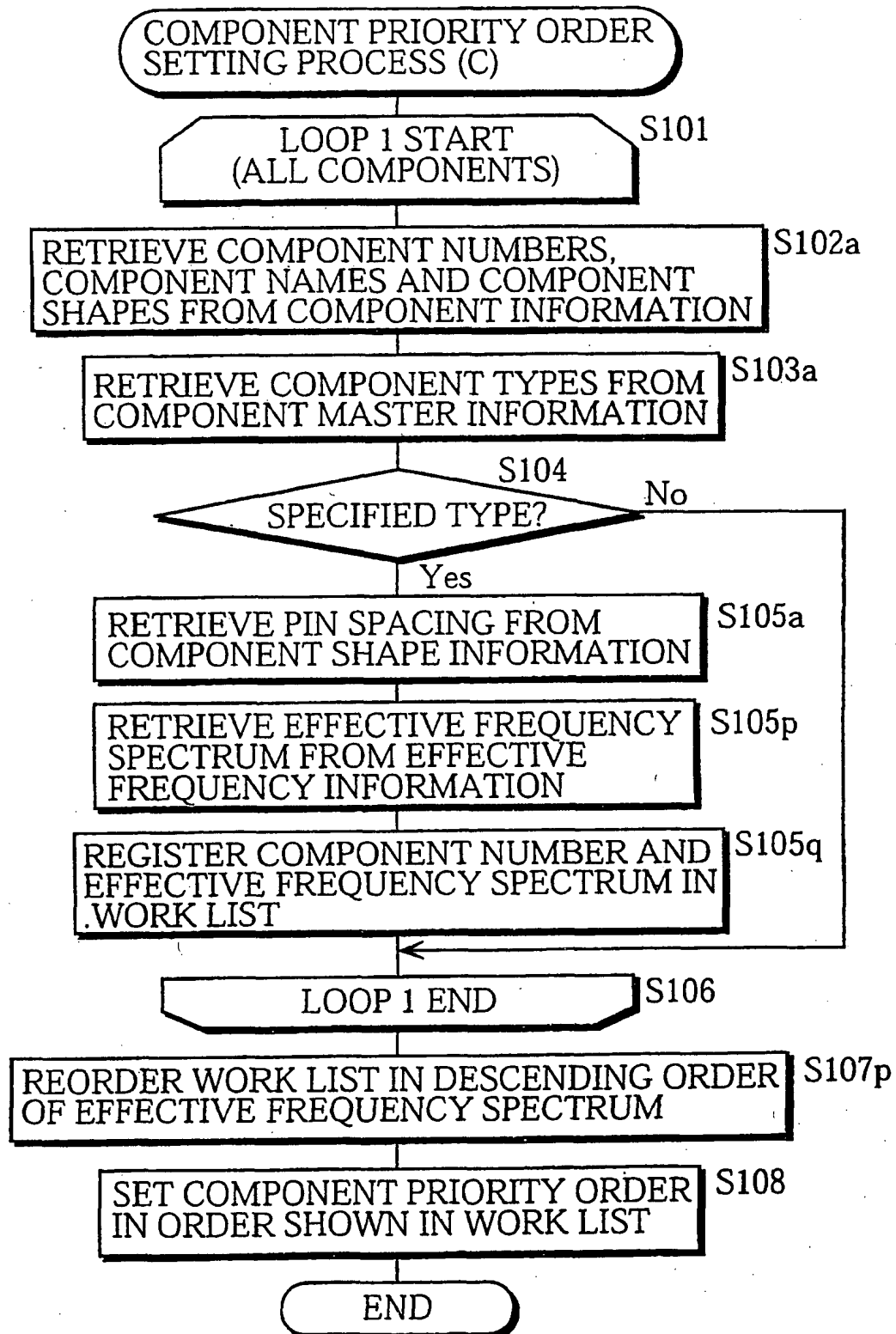


FIG. 14

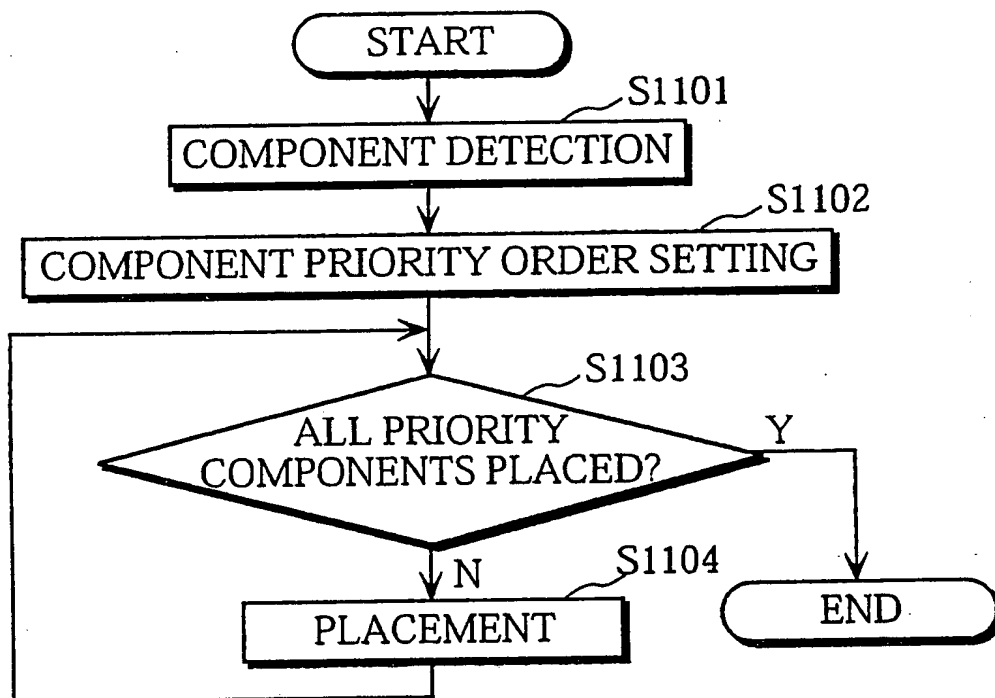


FIG. 15

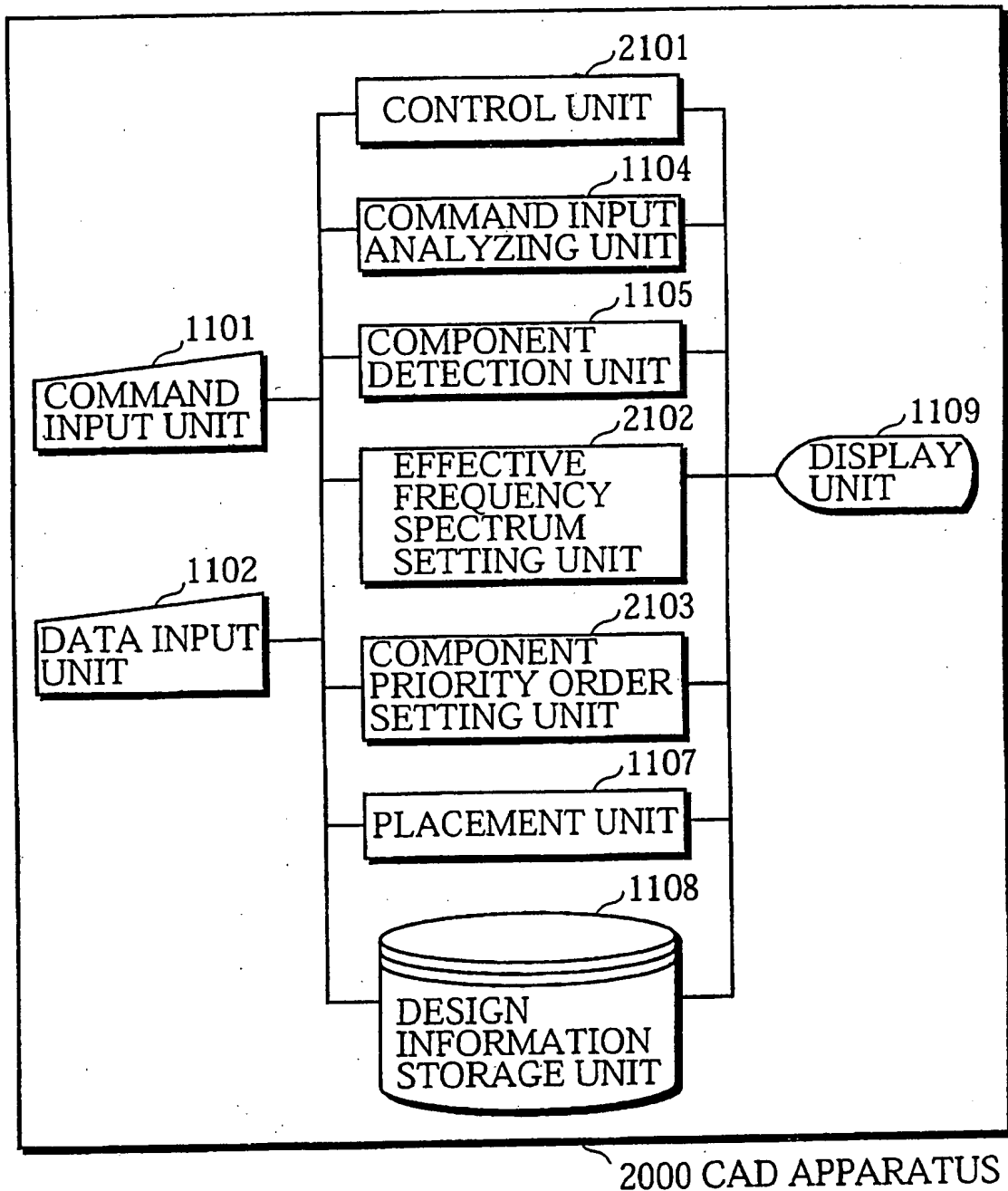


FIG. 16

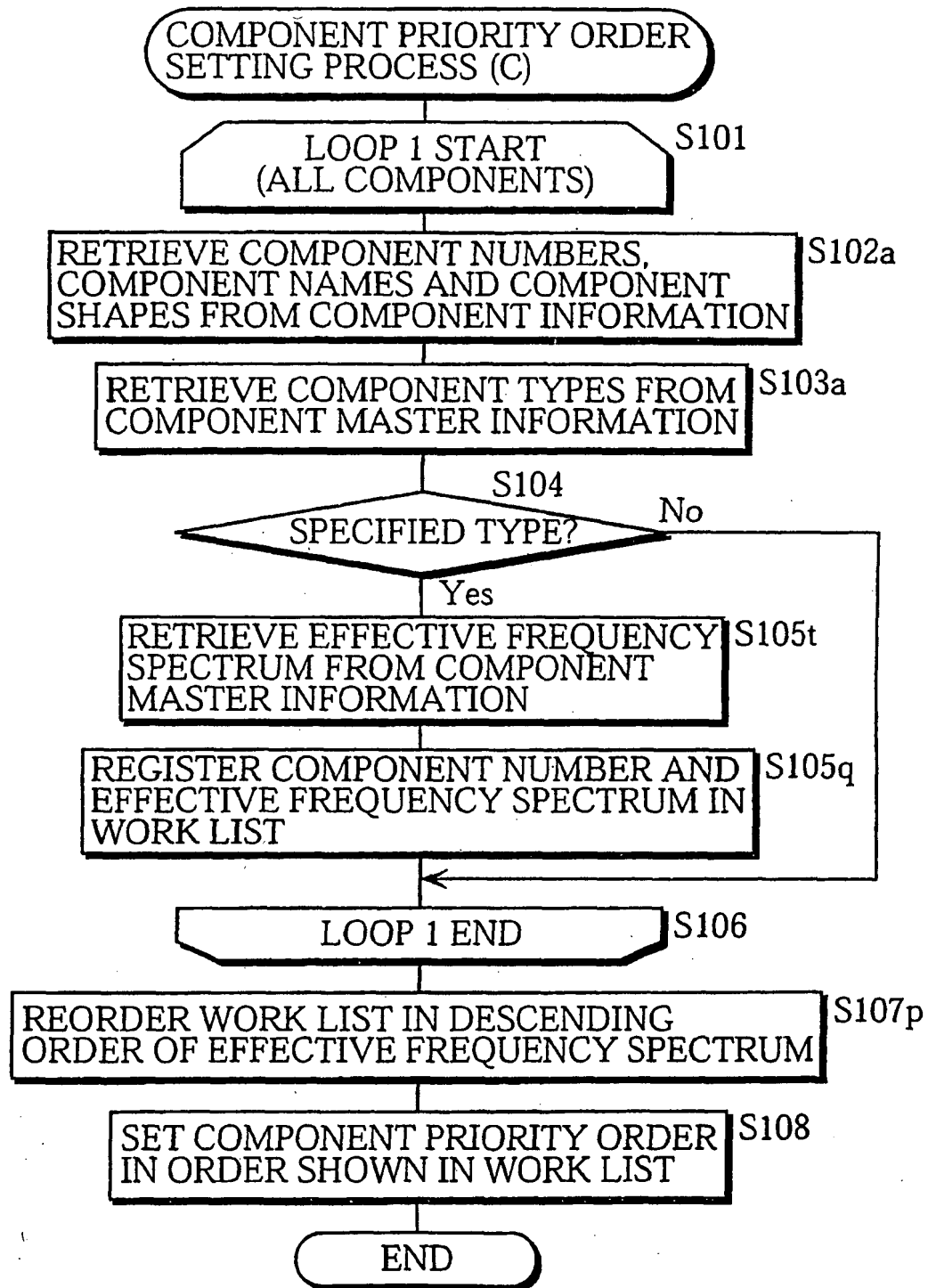


FIG. 17

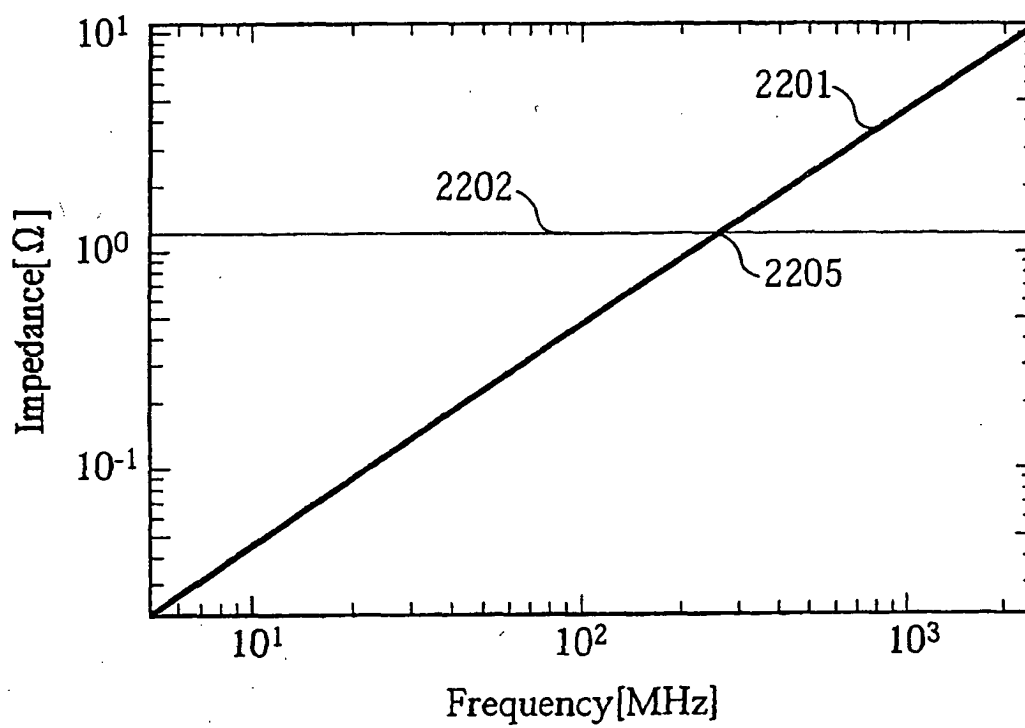


FIG. 18

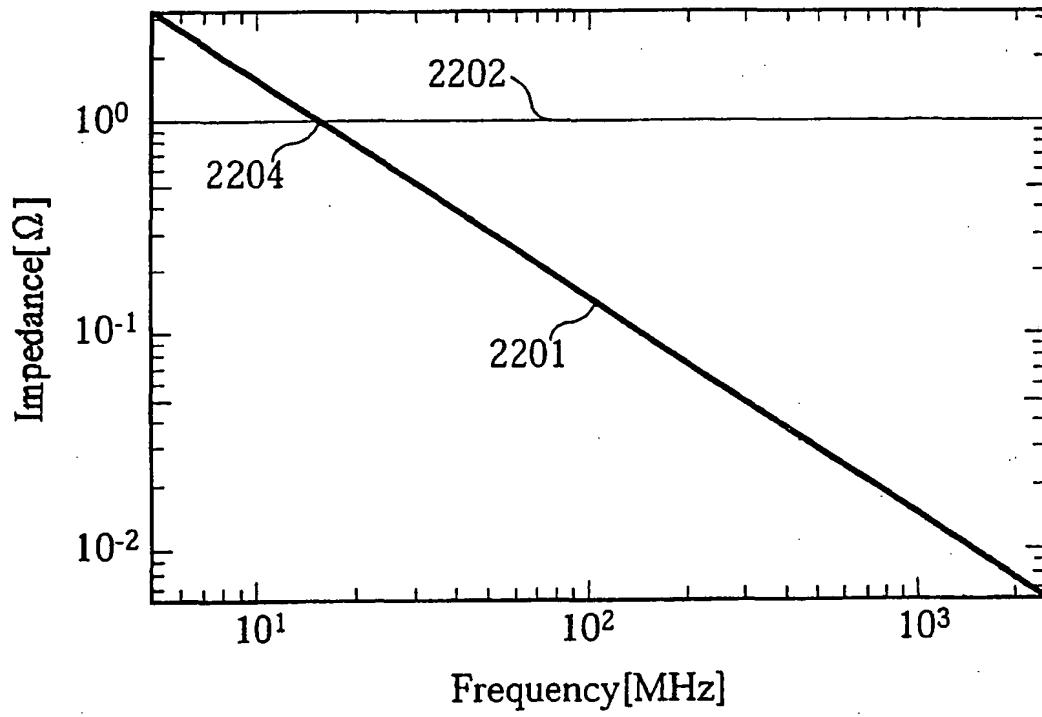


FIG. 19

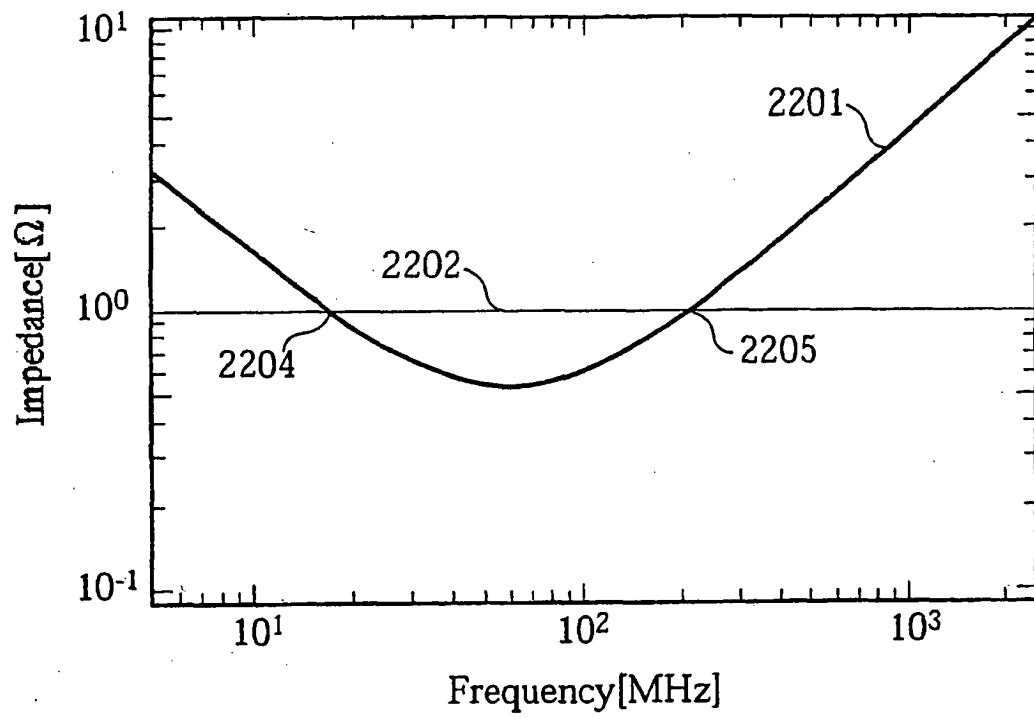


FIG. 20

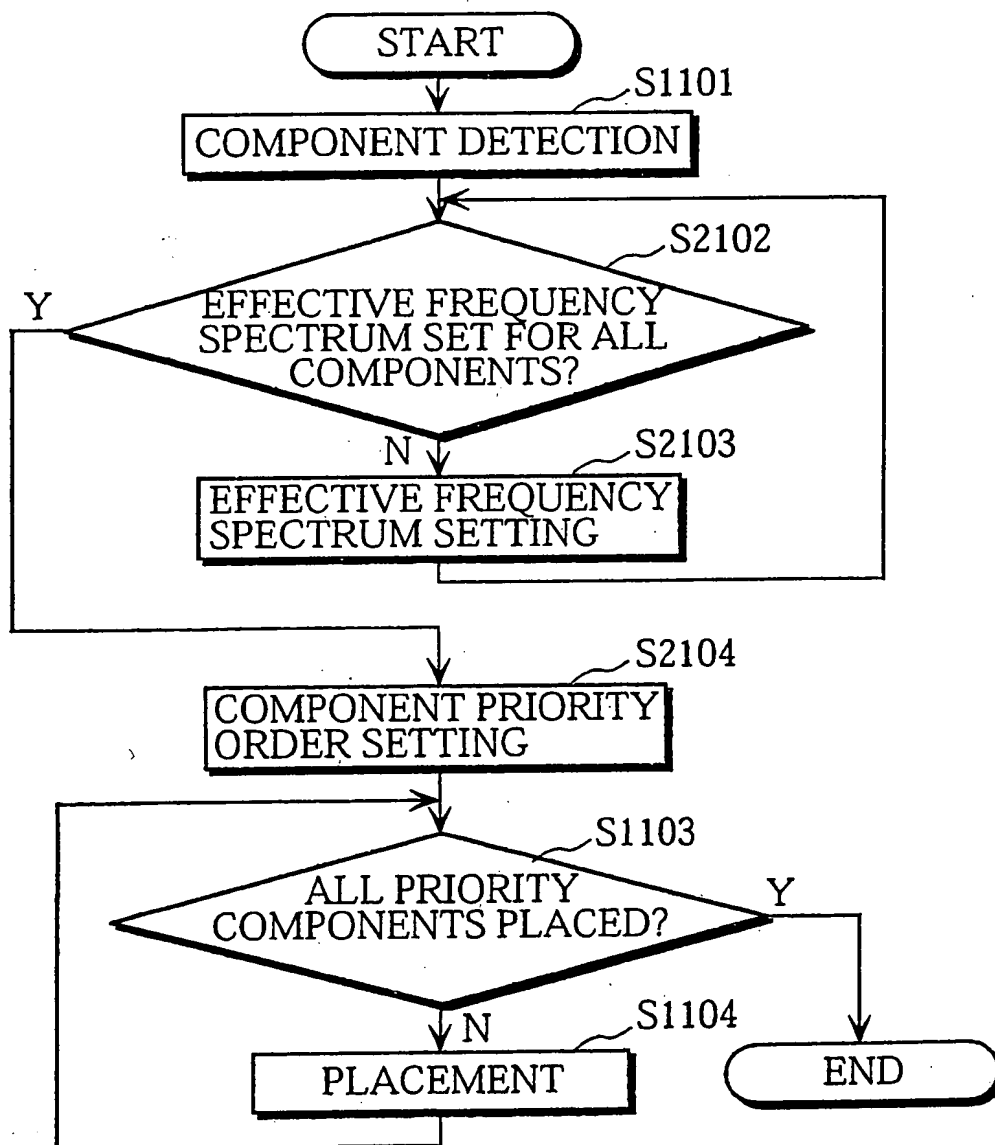


FIG. 21

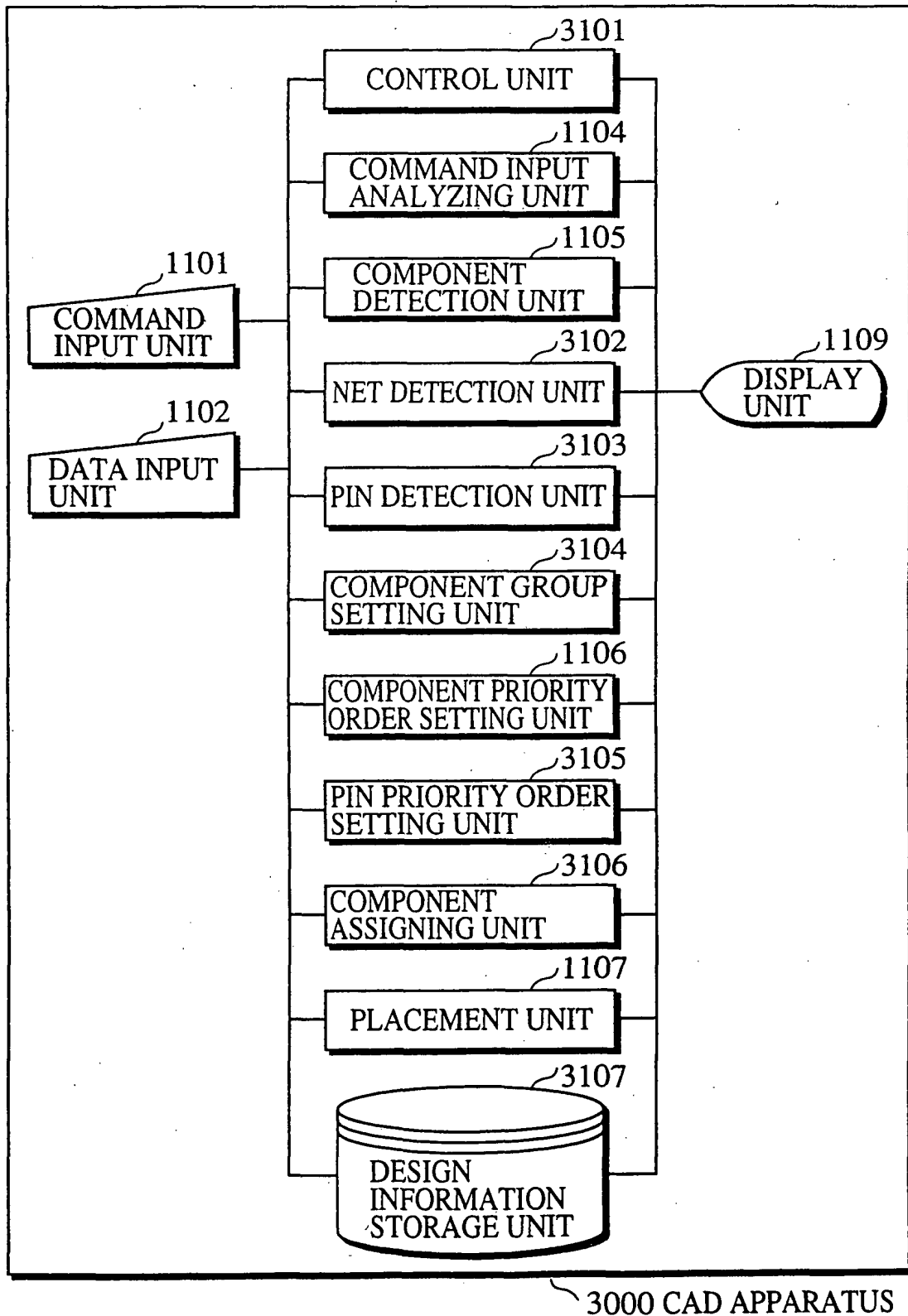


FIG. 22

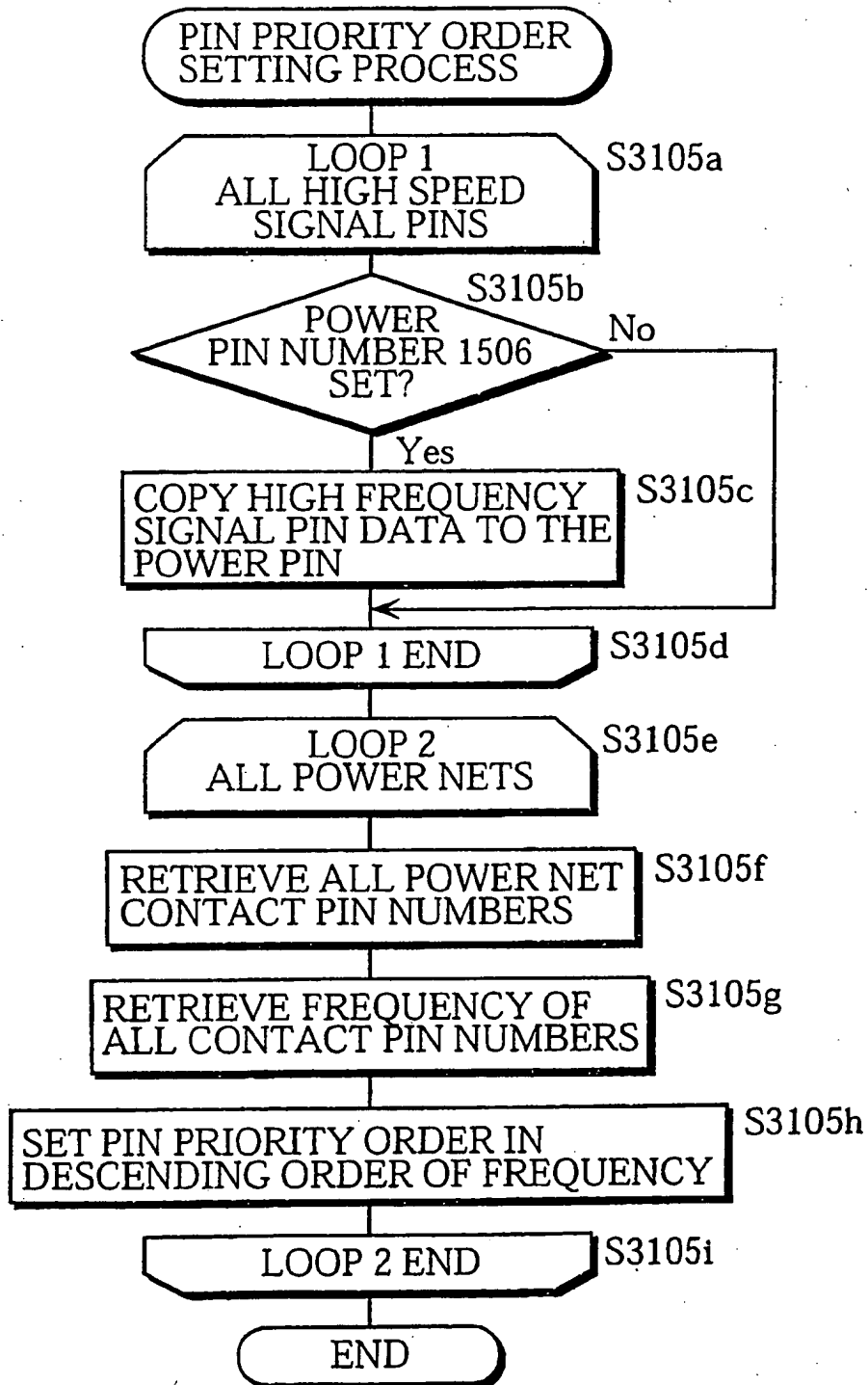


FIG. 23

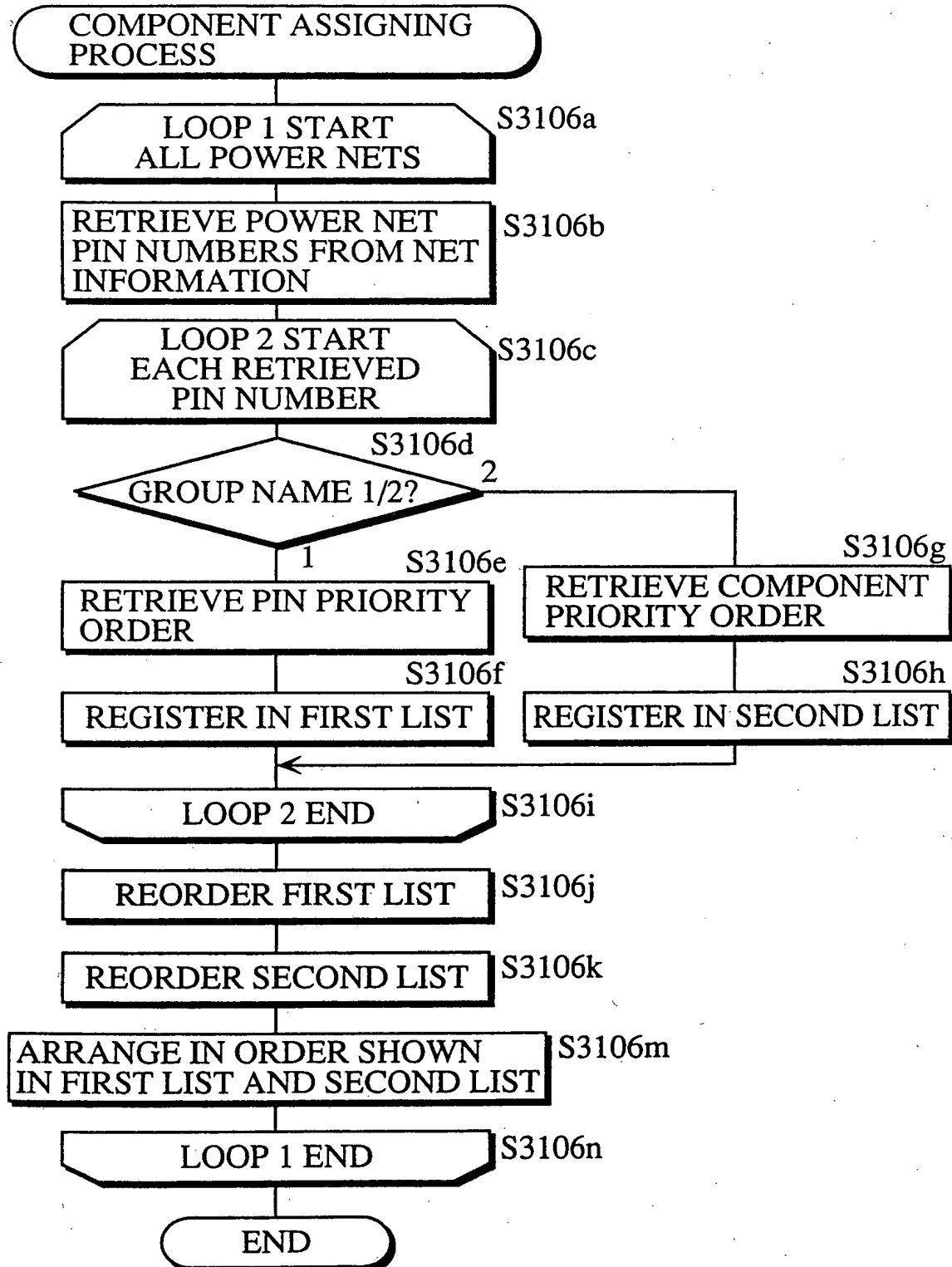


FIG. 24

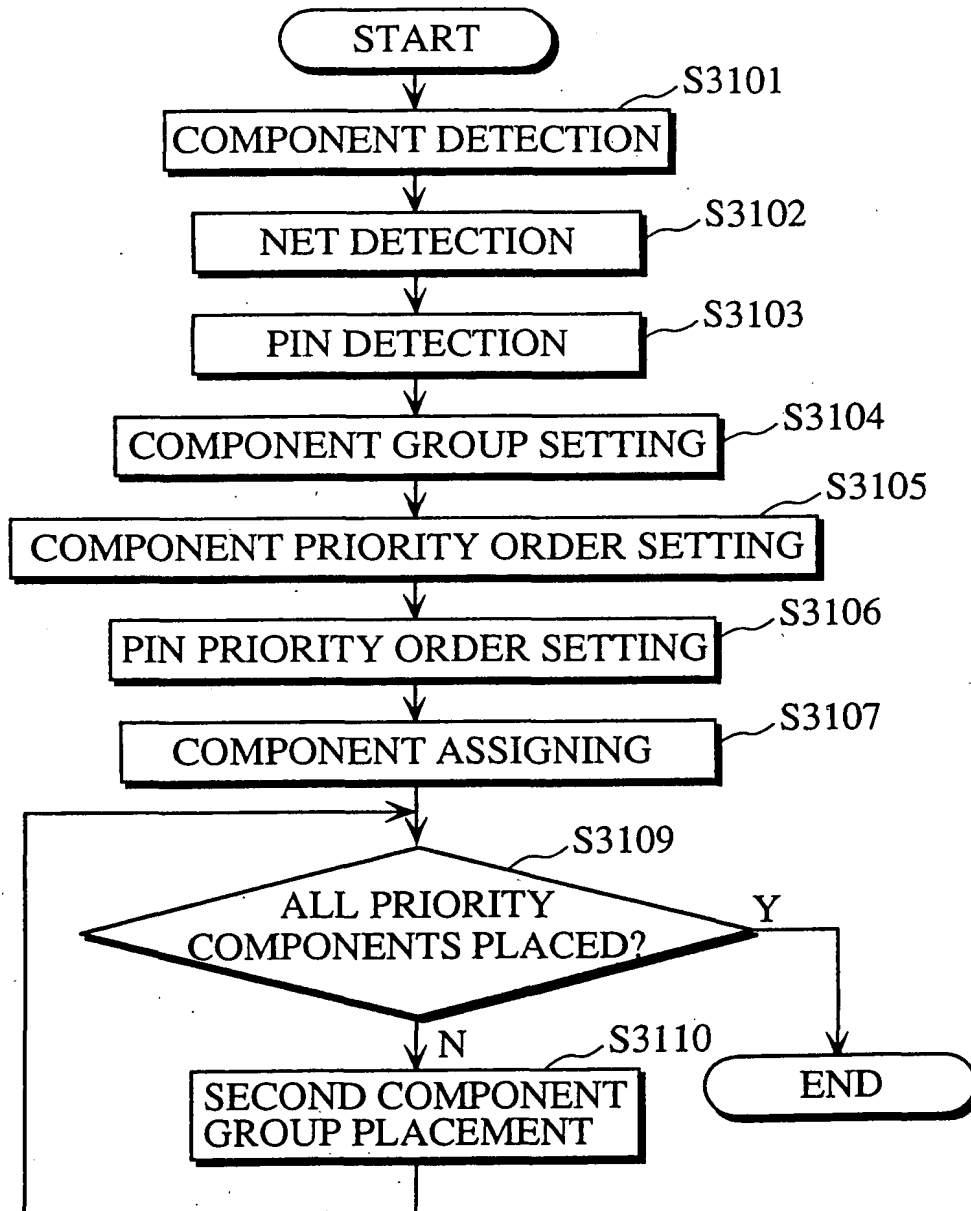


FIG. 25

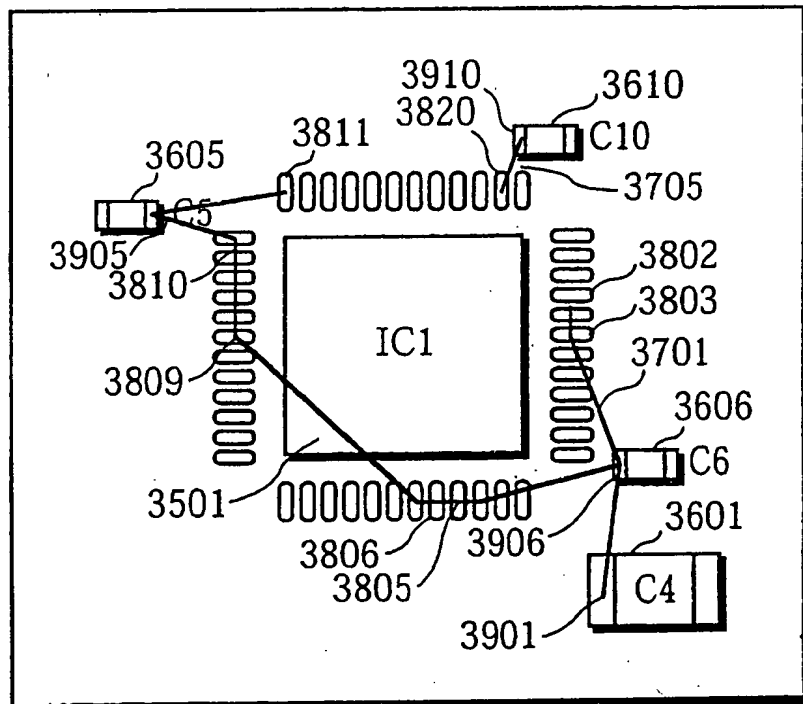


FIG. 26

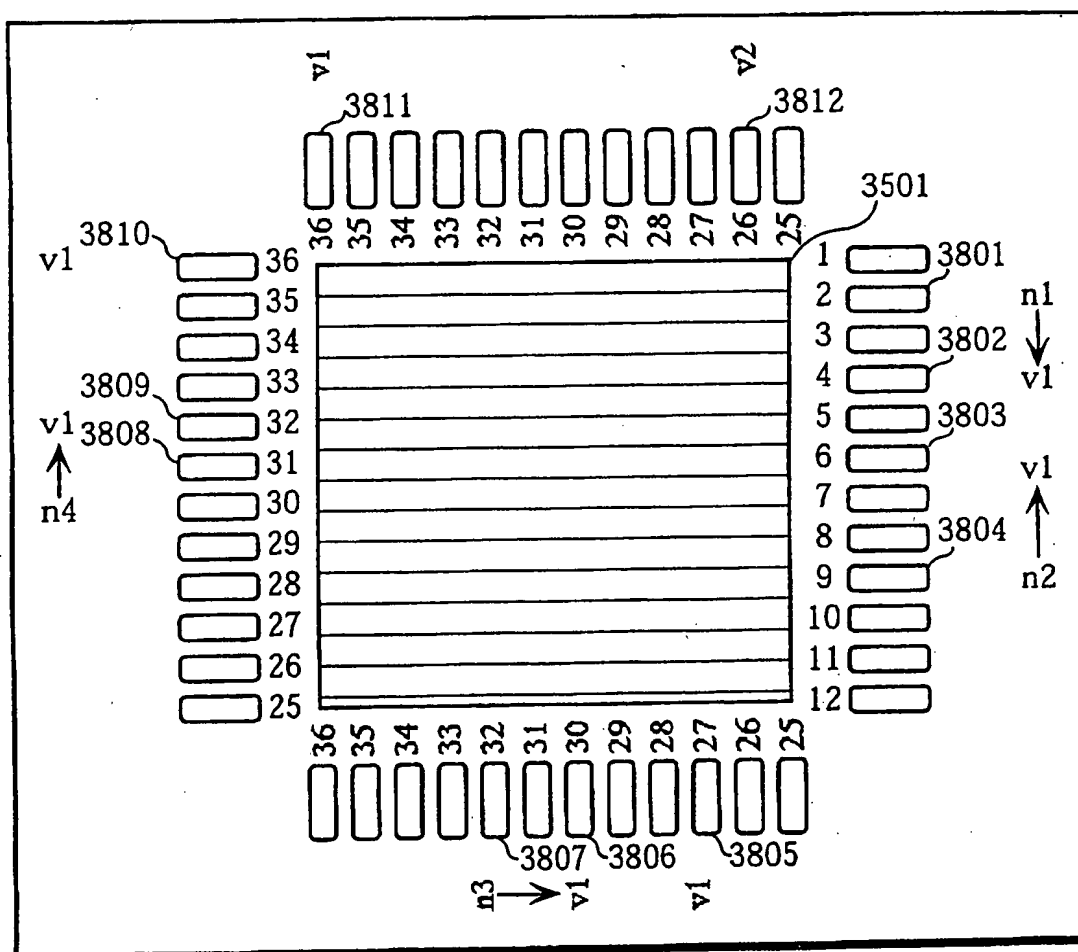


FIG. 27

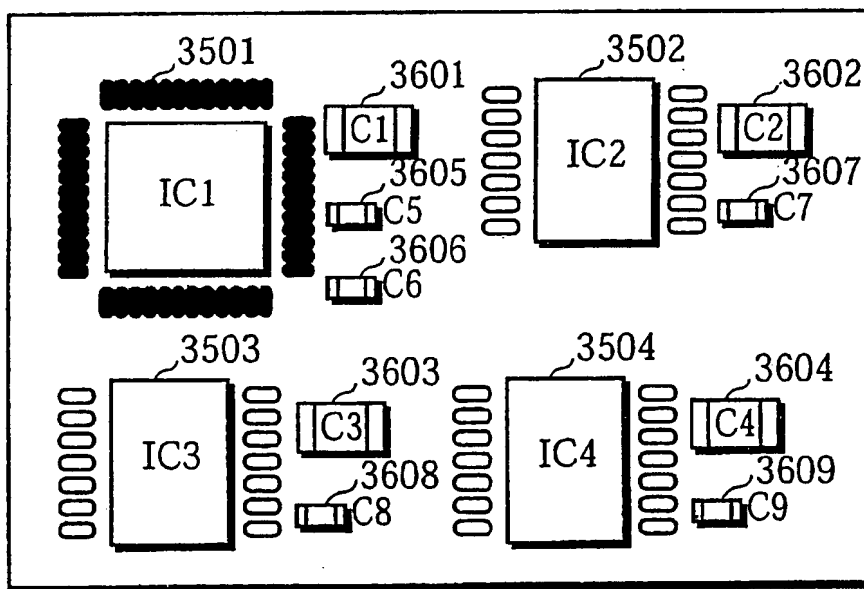


FIG. 28

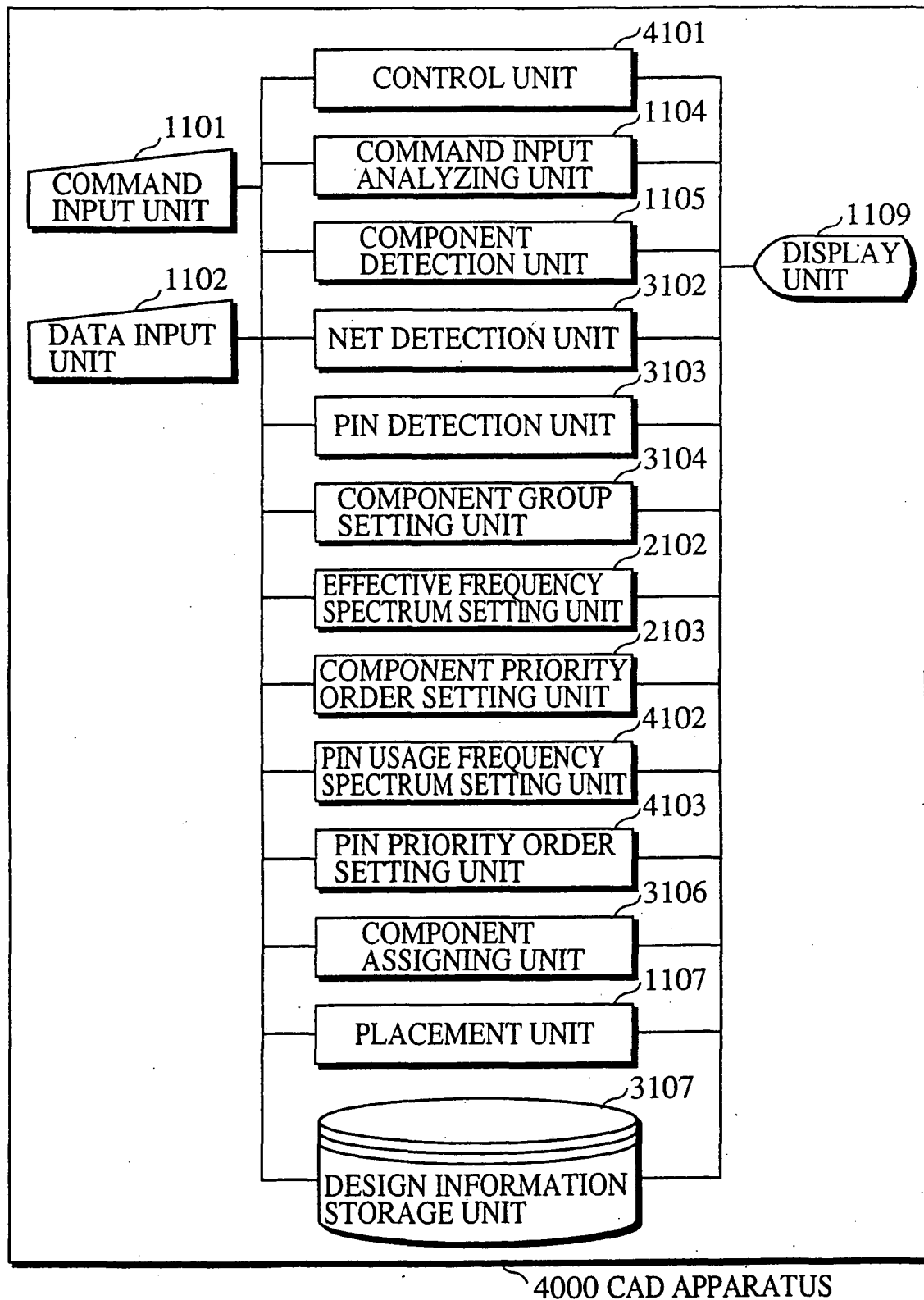


FIG. 29

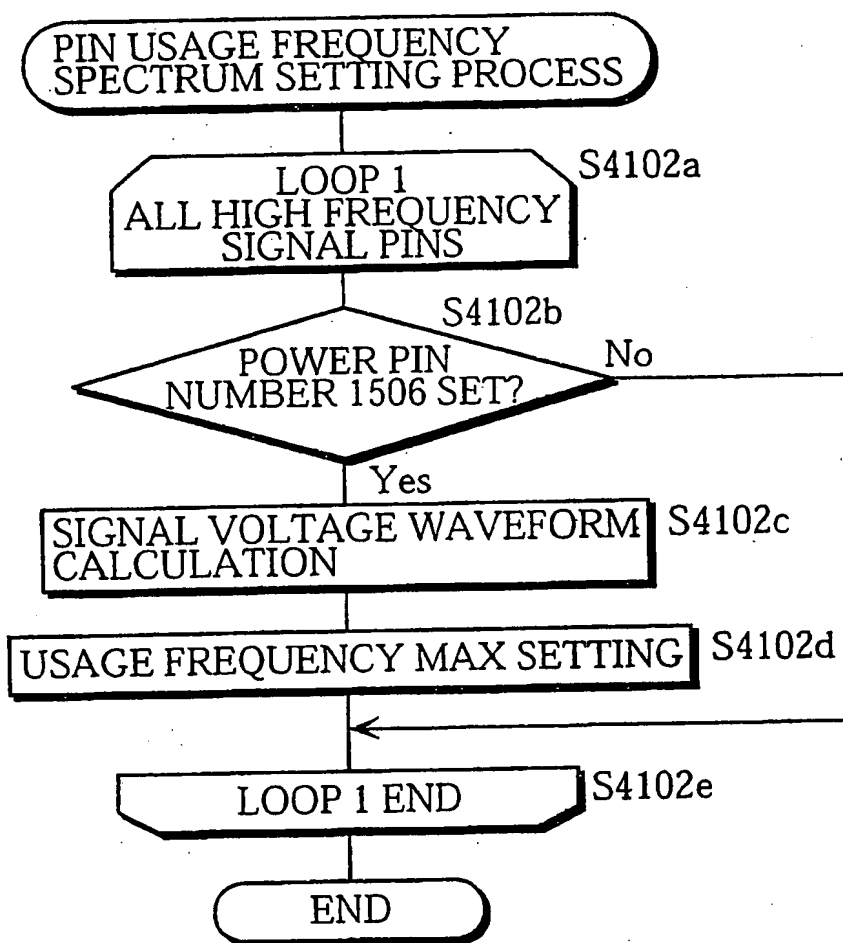


FIG. 30

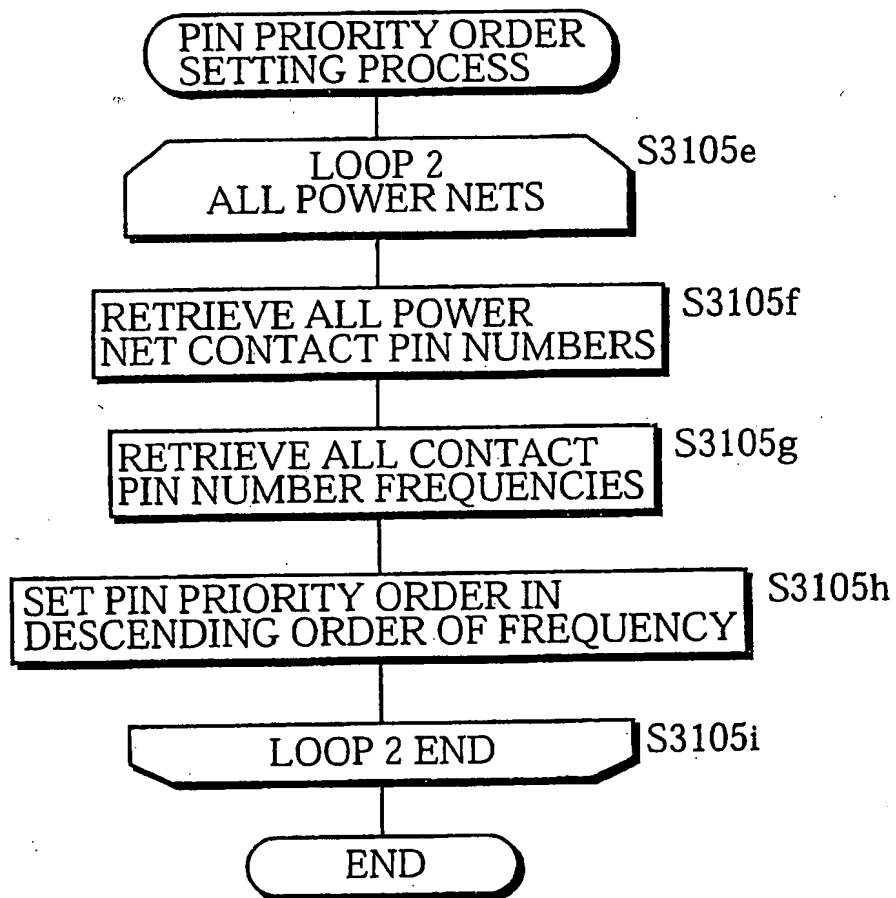


FIG. 31

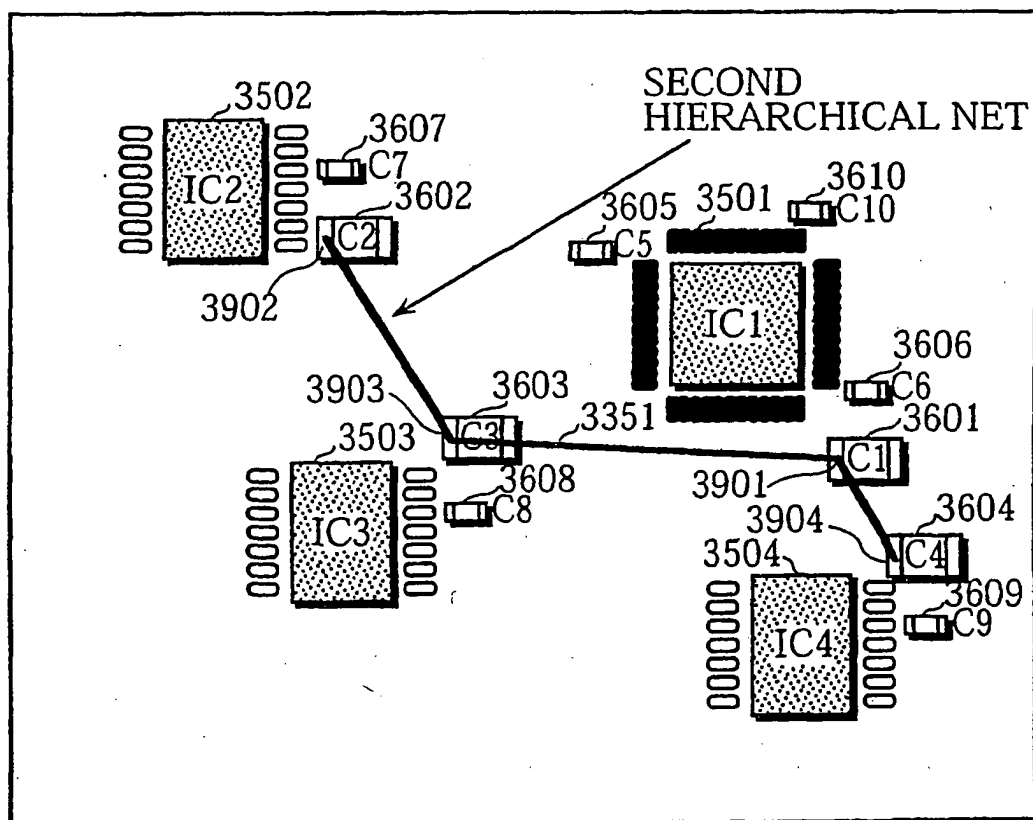


FIG. 32

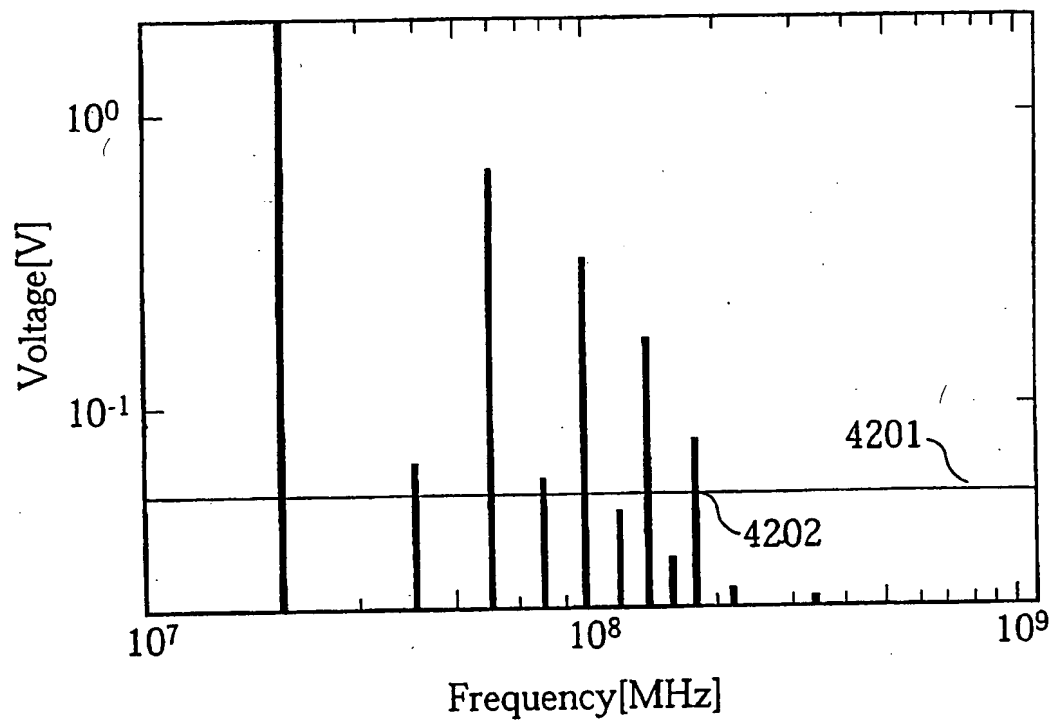


FIG. 33

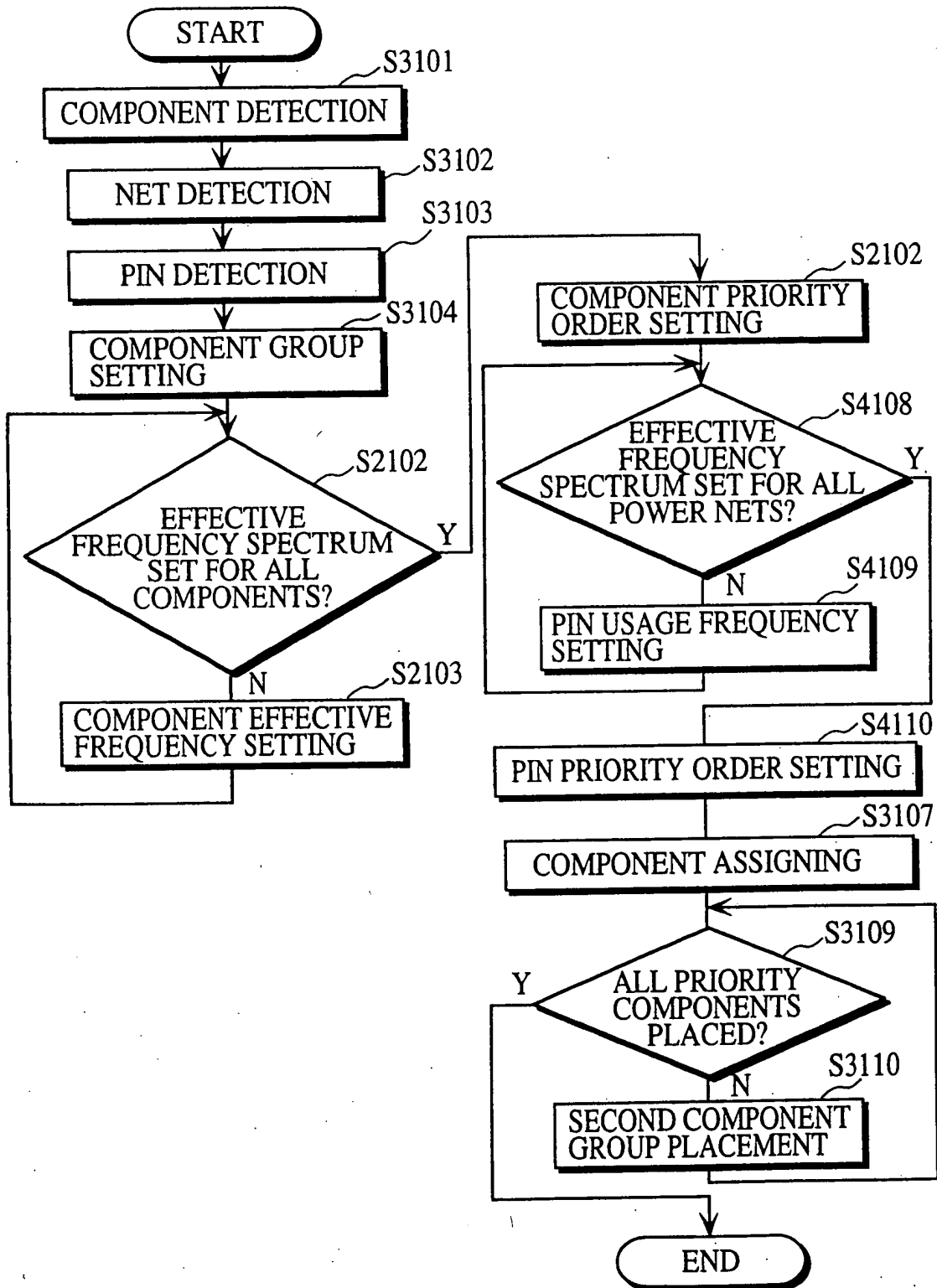


FIG. 34

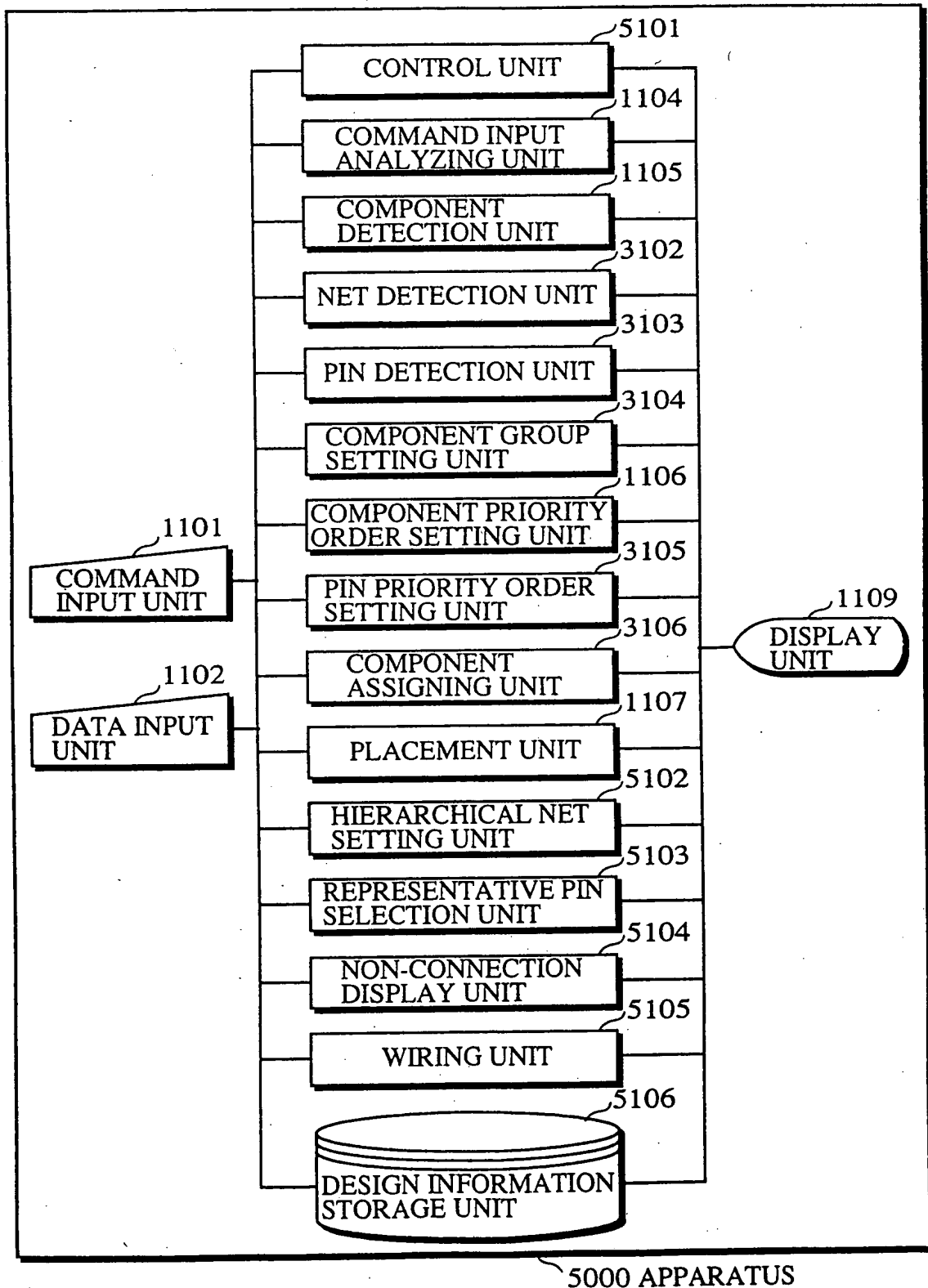


FIG. 35

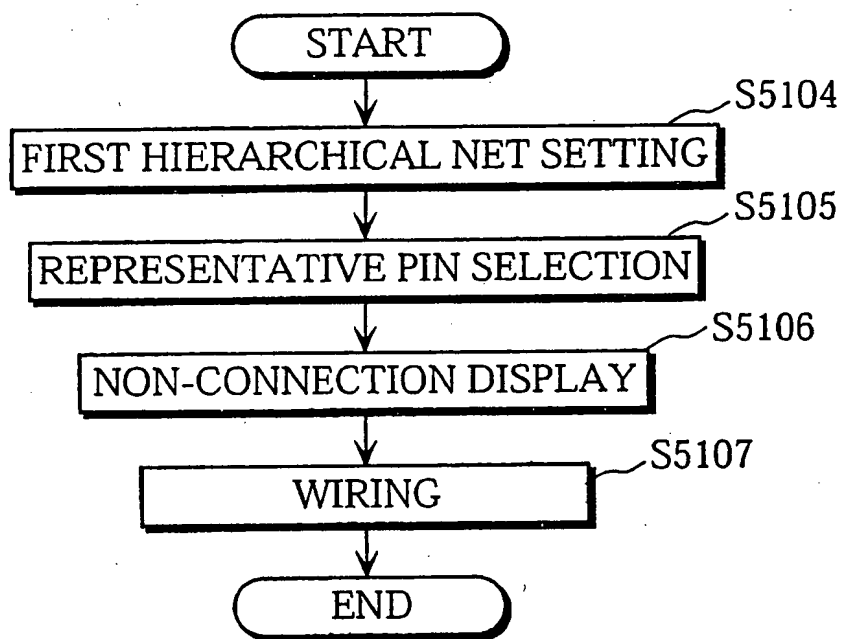


FIG. 36

1801 HIERARCHICAL NET INFORMATION LIST 1800

HIERARCHICAL NET INFORMATION				
1802	1803	1804	1805	1806
NET NAME	CONTACT PIN NUMBER (COMPONENT NUMBER-PIN NUMBER)	HIERARCHICAL NET NUMBER	REPRESENTATIVE PIN NUMBER	HIERARCHICAL NET CONTACT PIN NUMBER (COMPONENT NUMBER-PIN NUMBER)
Vcc1	IC1-4, IC1-6, IC1-15, IC1-18, IC1-32, IC1-36, ... C1-1, C5-1, ... 37, IC2-6, IC2-11, IC2-14 ... C1-1, C2-1, C3-1, ...	1	C1-1	IC1-4, IC1-6, IC1-15, IC1-18, IC1-32, IC1-36, ... C1-1, C5-1, ...
		2	C2-1	IC2-6, IC2-11, IC2-14, C2-1, C7-1
	
Vcc2	IC1-47, IC10-6, IC12-15, ... C10-1, C21-1, C23-1, ...	1	C10-1	IC1-47, C10-1
	
...

1822

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FIG. 37

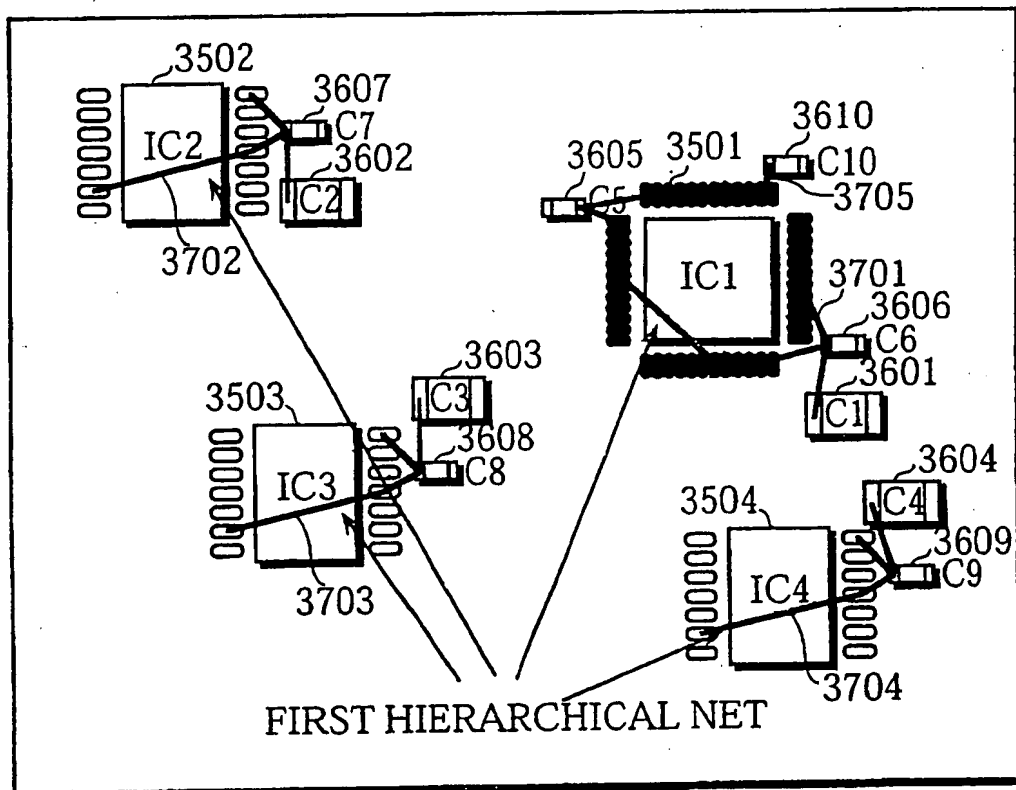


FIG. 38

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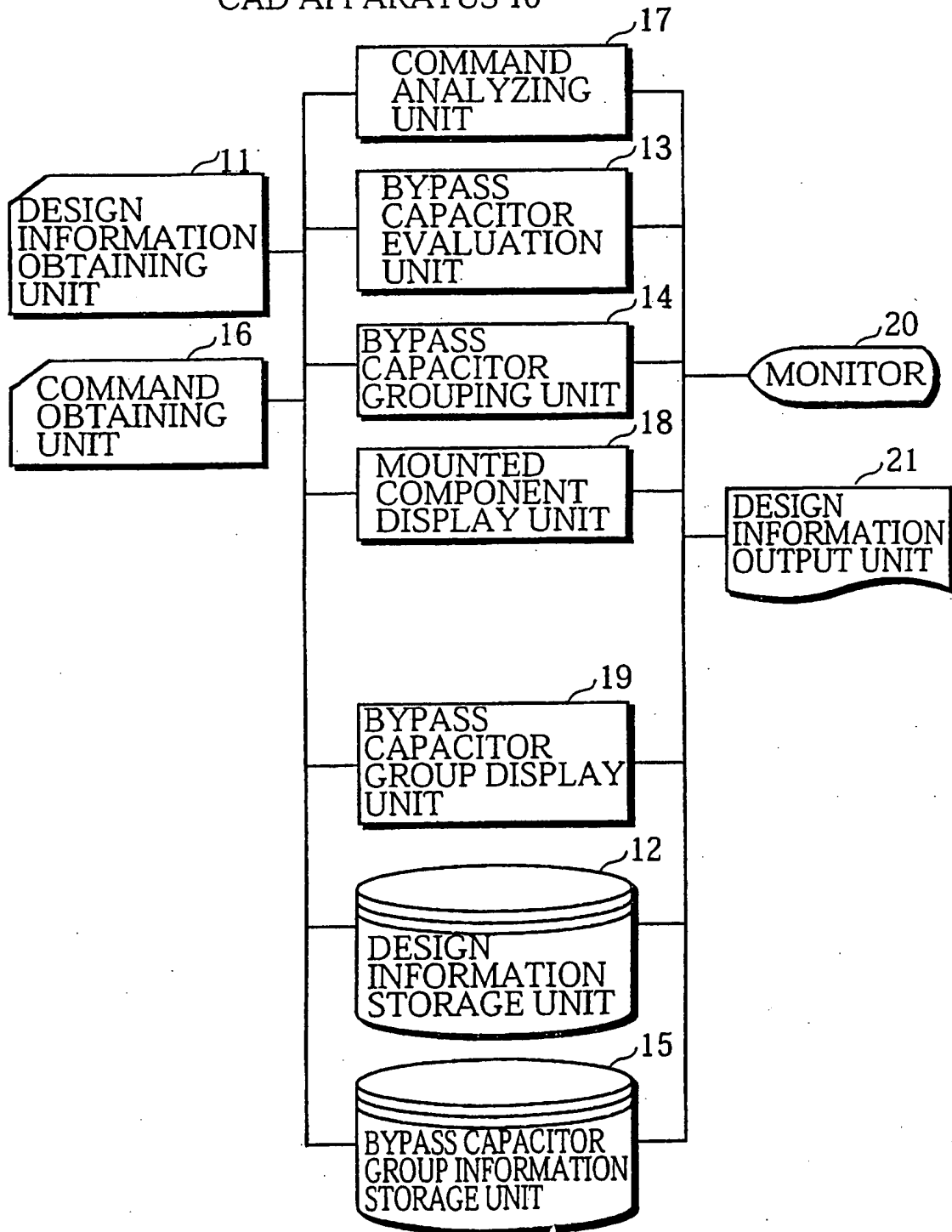


FIG. 39A

COMPONENT INFORMATION

COMPONENT NUMBER	COMPONENT NAME	COMPONENT TYPE	CAPACITY [μ F]	INDUCTANCE [nH]	EFFECTIVE PIN COUNT (NUMBER OF PINS)	REPRESENTATIVE POINT COORDINATES	MINIMUM / MAXIMUM DOMAIN
IC1	MN1	IC	—	—	—	(64,11)	(56,10) · (72,30)
IC2	MN2	IC	—	—	—	(84,11)	(76,10) · (92,30)
...	—	—	—
C1	EC10	CAPACITOR	0.1	0.5	3	(139,59)	(137,59) · (141,60)
C2	EC20	CAPACITOR	0.1	0.5	3	(150,59)	(148,59) · (152,60)
...

FIG. 39B

PIN INFORMATION

COMPONENT NUMBER	PIN NUMBER	NET NAME	NET TYPE	FREQUENCY [MHz]	NECESSARY CAPACITY [μ F]	REPRESENTATIVE POINT COORDINATES
IC1	1	PWR1	POWER	100	0.03	(69,29)
	2	GND1	GROUND	100	0.05	(69,11)
	3	CLK	CLOCK	100	0.01	(59,11)
	4	SIG1	GENERAL	100	0.01	(59,29)

...
C1	1	PWR1	POWER	—	—	(138,59)
C1	2	GND1	GROUND	—	—	(140,59)
C2	1	PWR2	POWER	—	—	(139,59)
C2	2	GND2	GROUND	—	—	(151,59)
...

FIG. 39C

NET INFORMATION

NET NAME	COMPONENT NUMBER	PIN NUMBER
GND1	IC1	2
	C1	2

GND2	C2	2

PWR1	IC1	1

FIG. 40

GROUP NUMBER	IC		BYPASS CAPACITOR		EFFECTIVENESS
	COMPONENT NUMBER	PIN NUMBER	COMPONENT NUMBER	PIN NUMBER	
1	IC1	4	C1	1	90
2	IC2	1	C2	1	70
3	IC3	1	C2	1	60
4	IC4	8	C3	1	50
5	IC4	8	C4	1	70
...

FIG. 41

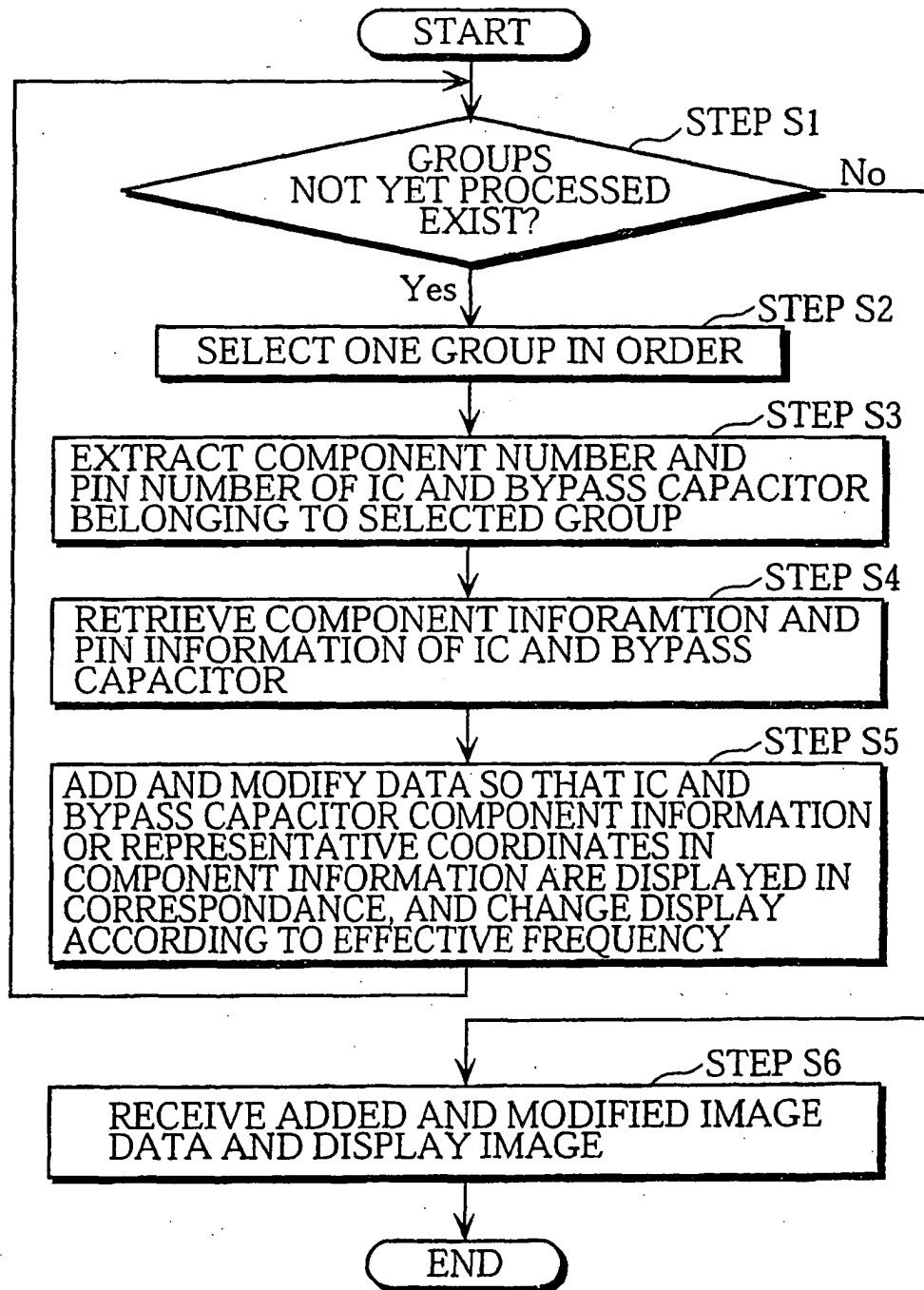


FIG. 42A

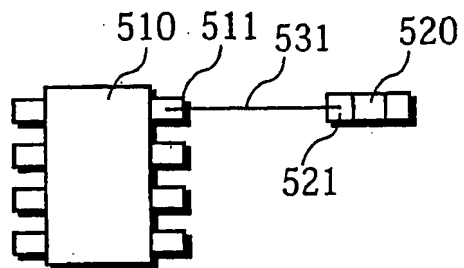


FIG. 42B

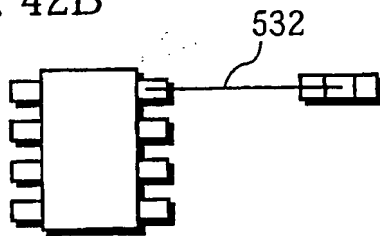


FIG. 42D

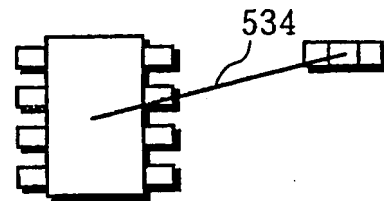


FIG. 42C

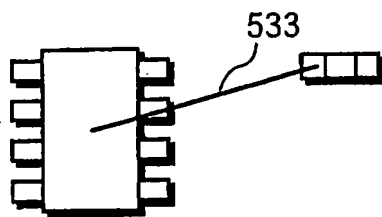


FIG. 43A

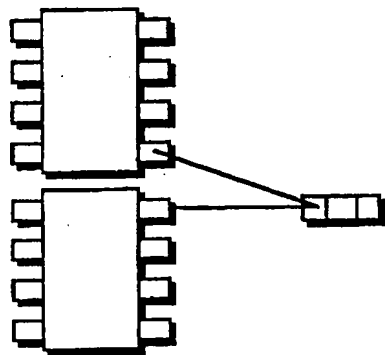


FIG. 43B

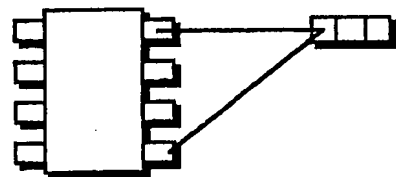


FIG. 43C

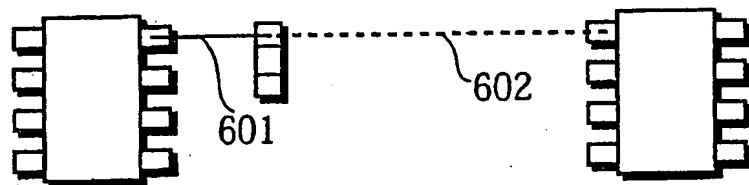


FIG. 44A

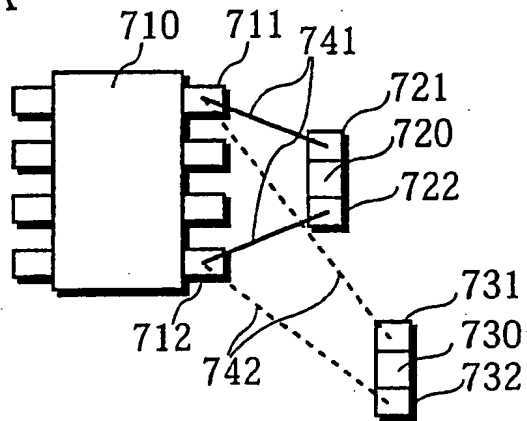


FIG. 44B

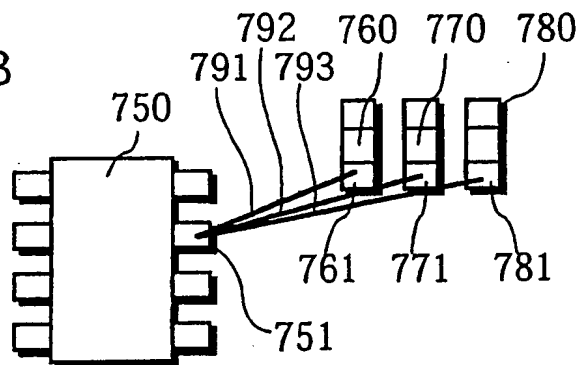


FIG. 45

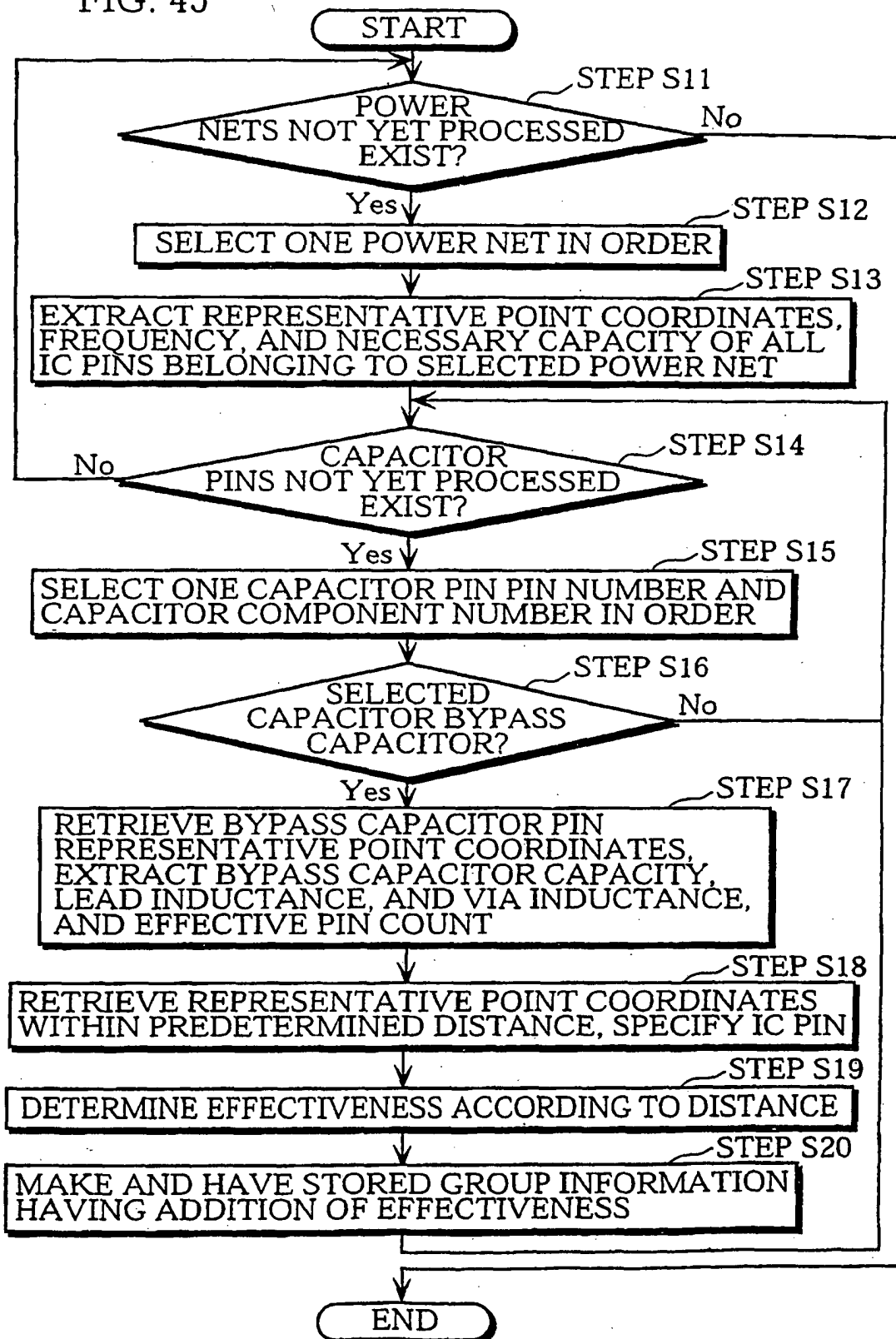


FIG. 46A

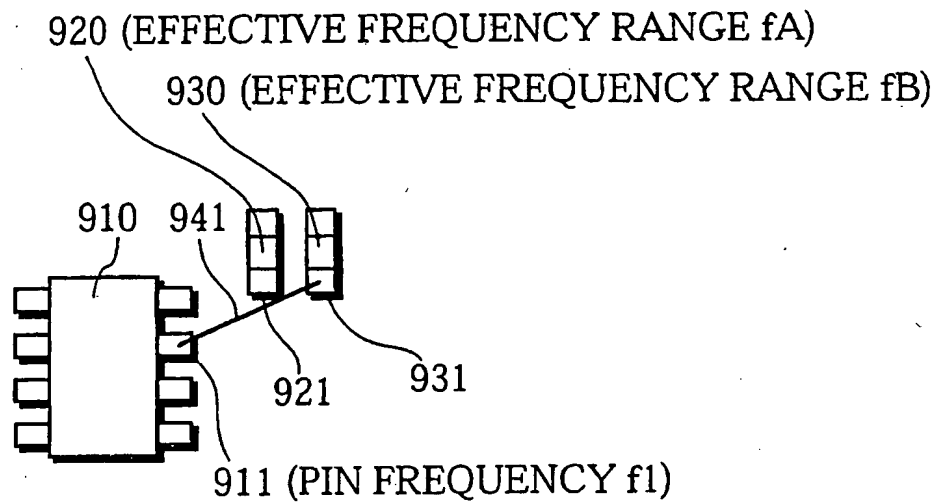


FIG. 46B

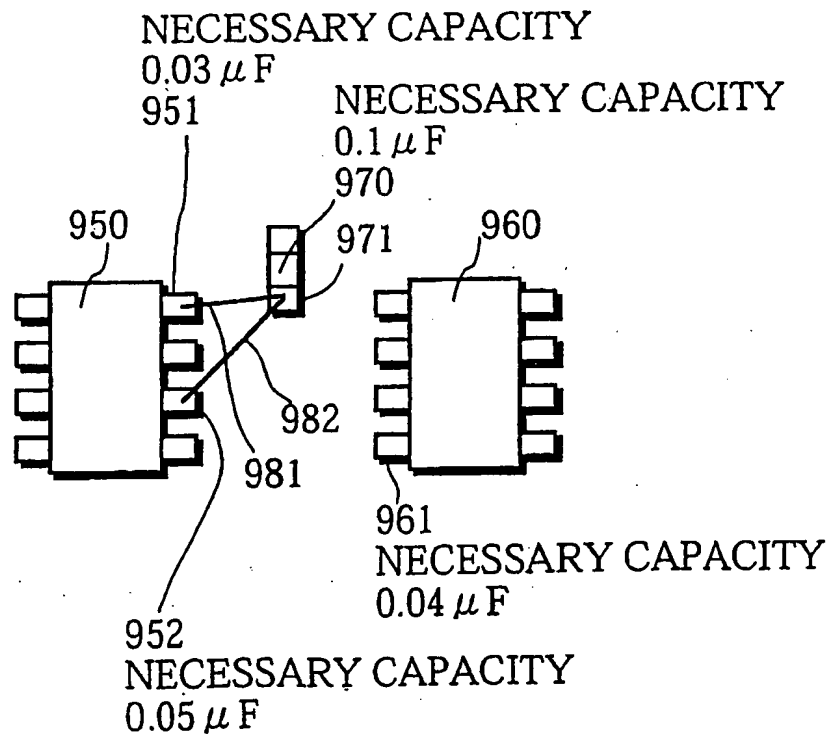


FIG. 47

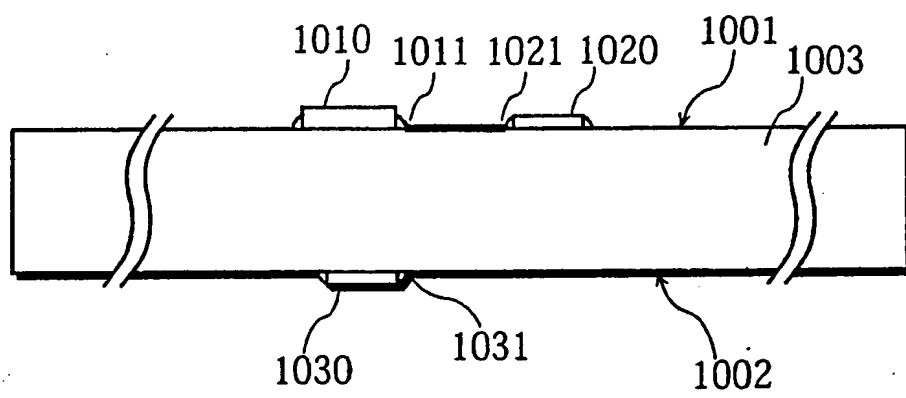


FIG. 48

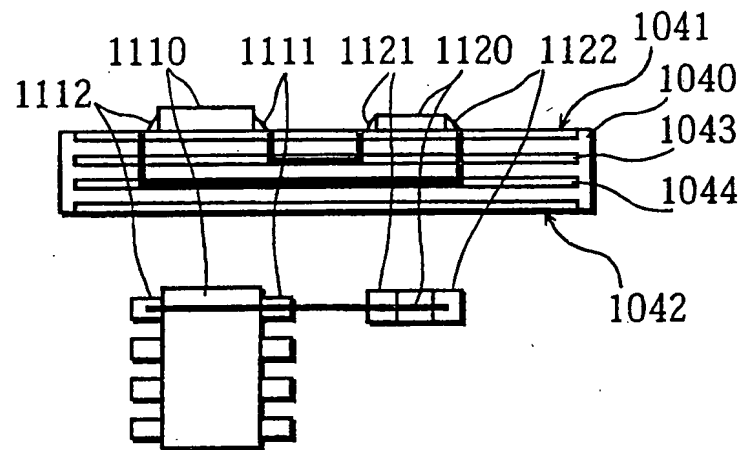


FIG. 49

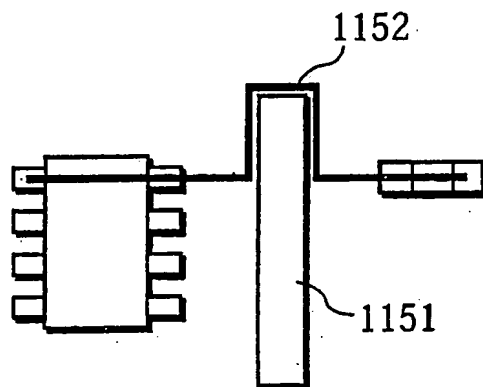


FIG. 50

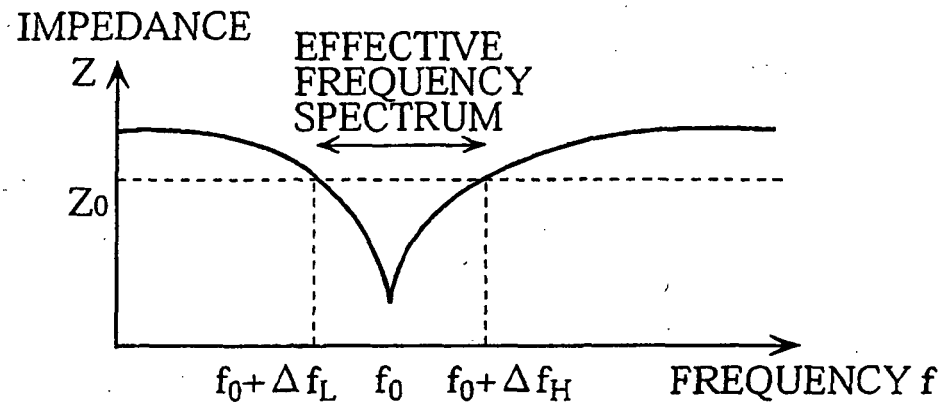


FIG. 51A

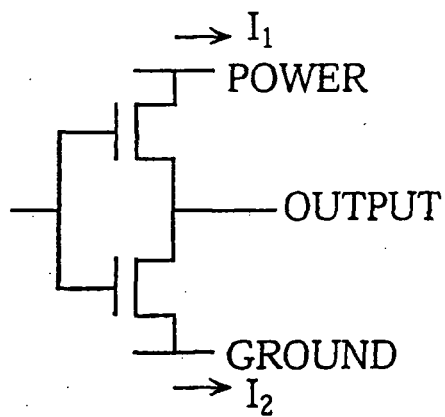


FIG. 51B

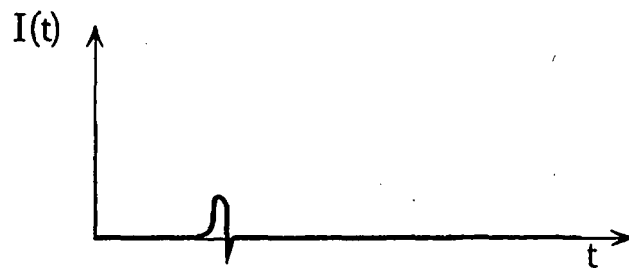


FIG. 51C

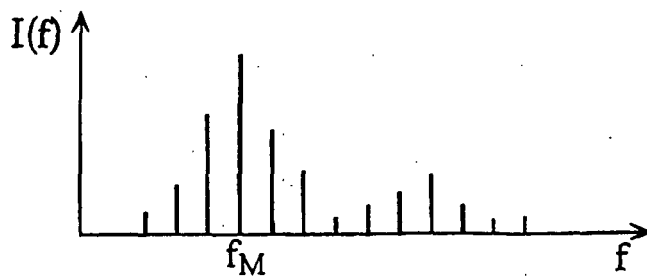


FIG. 52

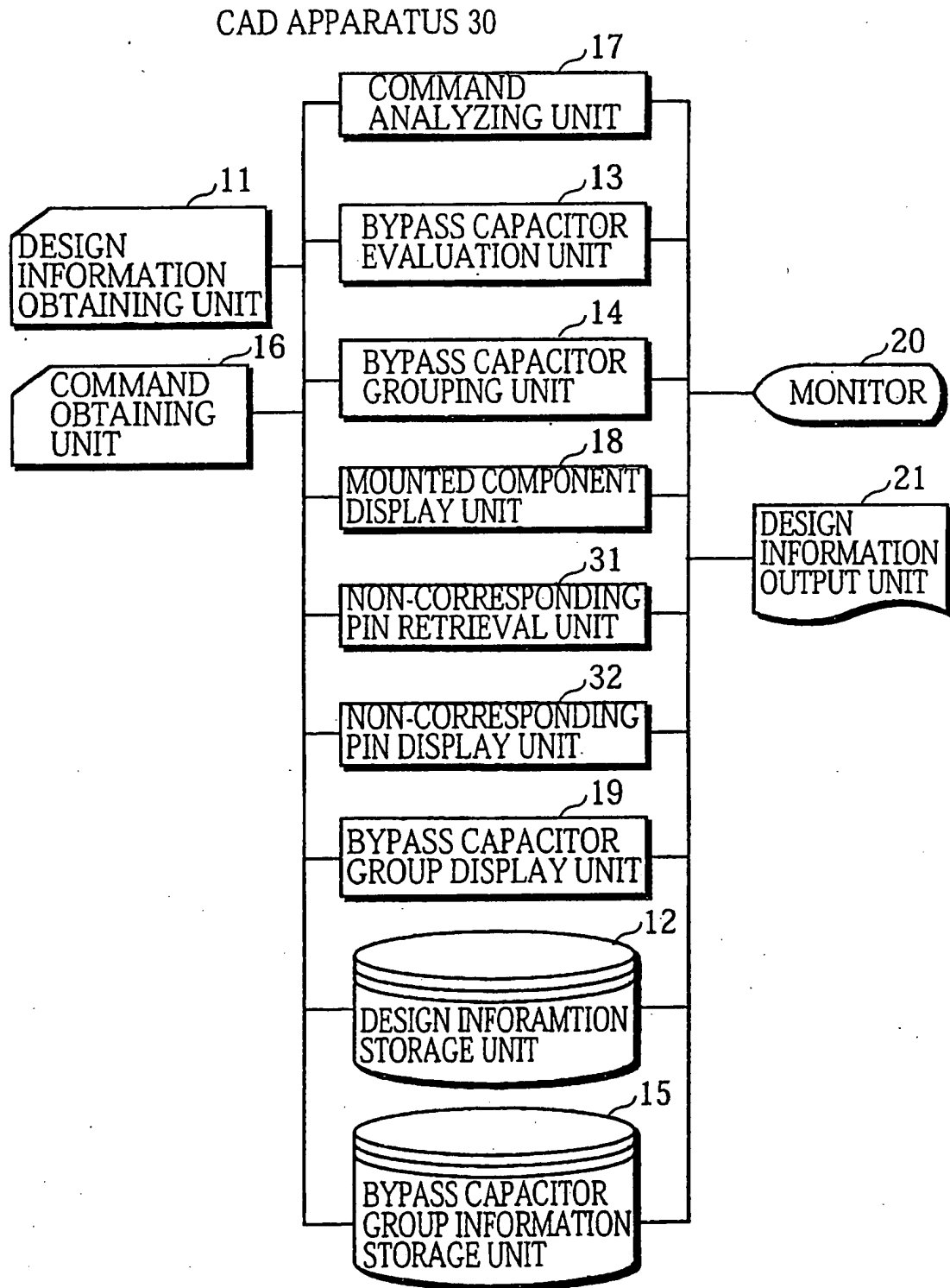


FIG. 53

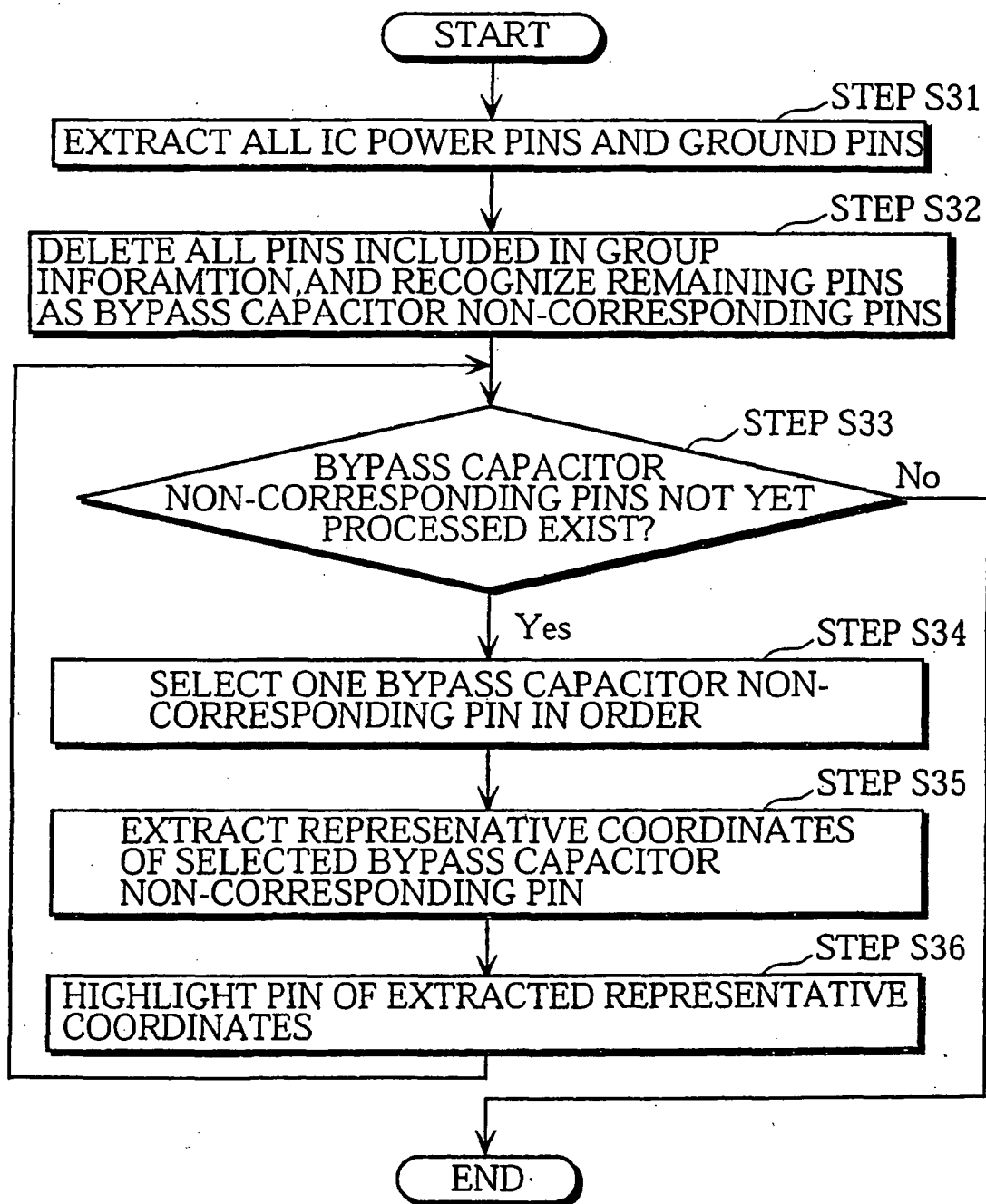


FIG. 54

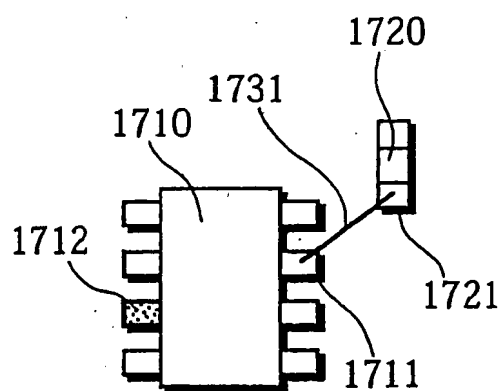


FIG. 55

CAD APPARATUS 40

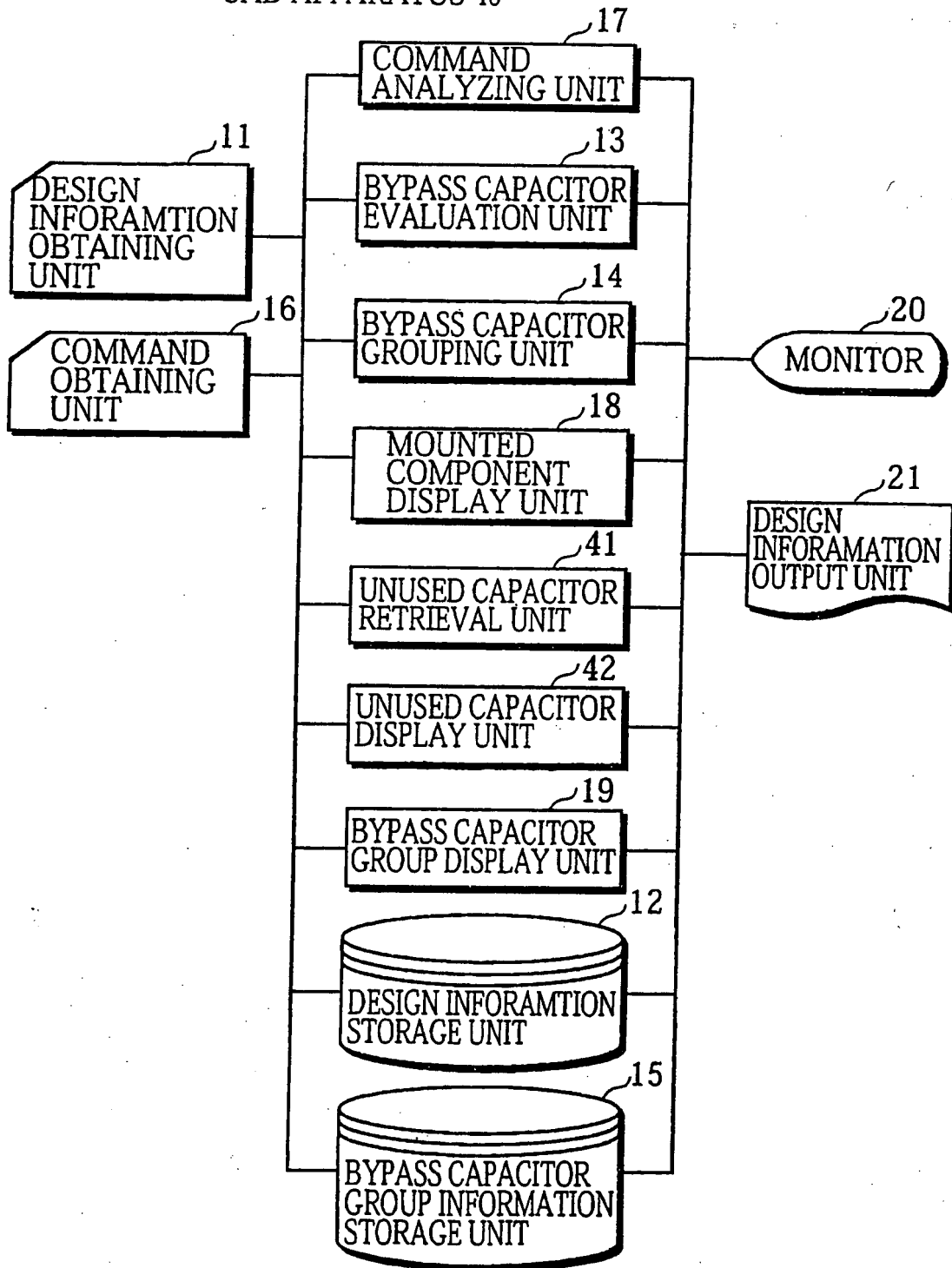


FIG. 56

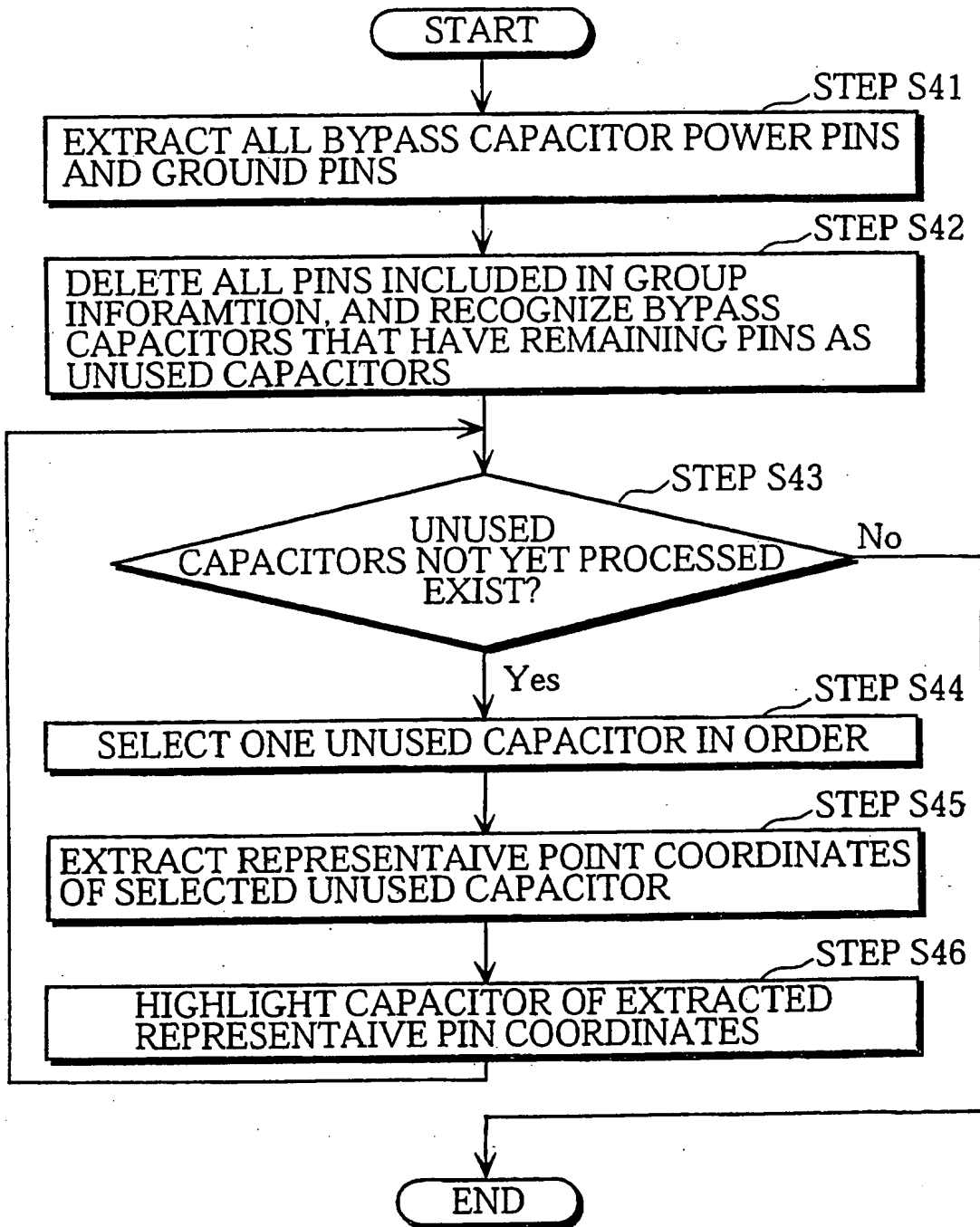


FIG. 57

